Department of Information Technology and
Electrical Engineering

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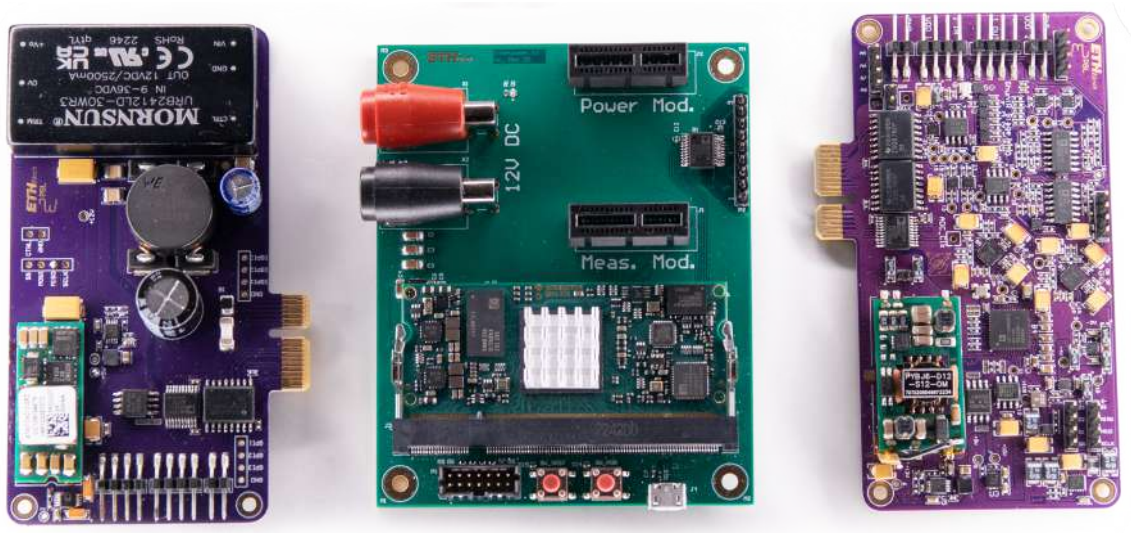
Design and Validation of a Combined Power Tracer and Sensor Emulator for the Evaluation of Embedded Hardware/Software System Designs

Master Thesis



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Abstract

This report presents the development of a novel hardware in the loop testbed for embedded devices, capable of measuring a broad range of currents and voltages, providing power delivery, and enabling simultaneous stimulation and data recording for the device under test. The modular testbed comprises three primary components: the power profiler module, the power delivery module, and the data interposer module. By achieving a current measurement range of 210 dB and offering 20 W of power delivery to the DUT, this HIL testbed demonstrates a comprehensive solution for testing low-power devices and those requiring high inrush current, such as FPGAs. The modular design allows for easy expansion and adaptation to meet the evolving needs of modern embedded systems and serves as a foundation for future work and development in the field.

Declaration of Originality

I hereby confirm that I am the sole author of the written work here enclosed and that I have compiled it in my own words. Parts excepted are corrections of form and content by the supervisor. For a detailed version of the declaration of originality, please refer to Appendix C

Nando Galliard,
Zurich, March 2023

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List of Acronyms

ADC . . . . . .analog to digital converter
ADS . . . . . .advanced design systems

CRC . . . . . .cyclic redundancy check

DIM . . . . . .data interposer module
DMA . . . . . .direct memory access
DUT . . . . . .device under test

EDA . . . . . .electronic design automation
EMC . . . . . .electromagnetic compatibility
ENOB . . . . . .effective number of bits
ESD . . . . . .electro static discharge

FIFO . . . . . .first in first out
FPGA . . . . . .field programmable gate array

HIL . . . . . .hardware in the loop

InAmp . . . . .instrumentation amplifier
IP . . . . . .intellectual property

LDO . . . . . .Low-dropout regulator

MOSFET . . . . metal oxide silicon field effect transistor

ODR . . . . . output data rate
OpAmp . . . . . operational amplifier

PDM . . . . . power delivery module
PL . . . . . programmable logic
PPM . . . . . power profiler module
PS . . . . . processing system
PSD . . . . . power spectral density

RF . . . . . radio frequency
RTL . . . . . register transfer level
RTOS . . . . . real time operating system

SINAD . . . . . signal to noise and distortion
SNR . . . . . signal to noise ratio
SoC . . . . . system on chip
SPI . . . . . serial peripheral interface

THD . . . . . total harmonic distortion

Chapter 1

Introduction

For any scientific report, the reproducibility of an experiment is one of the critical pillars on which the scientific community stands. In the field of embedded devices, it has always been a challenging endeavour to reproduce stimulus with timing in the nanoseconds. Additionally, an embedded device typically consists of tens to thousands of components interacting with each other. The primary objective of a hardware in the loop (HIL) testbed is to strip away all this complexity and precisely interact with only the desired component. To meet these challenges, this report presents the development of a HIL testbed which not only measures current with a novel analogue feedback circuit capable of reaching a current range of 210 dB, significantly enhancing the precision and sensitivity of measurements while also providing power delivery up to 10A to satisfy inrush currents from FPGAs while simultaneously stimulating and recording data for the embedded DUT.

The HIL testbed comprises three primary modular components: the power profiler module (PPM), the power delivery module (PDM), and the data interposer module (DIM). The PPM employs the novel method for measuring a wide range of currents by a feedback loop of a variable shunt resistance controlled by a cascade of hysteresis analogue circuits. An autonomous high-power mode can additionally halt this hysteresis. This system achieves a current measurement range from 310 pA to 10 A, significantly surpassing the performance of related work [2, 3]. The DUT can supply up to 20 W of power with high accuracy, offering a complete solution for a broad range of embedded device under test (DUT). The DIM enables interaction with multiple devices through the serial peripheral interface (SPI), ensuring reliable communication and isolation between the testbed and the DUT.

By combining advanced measurement techniques, power delivery capabilities, and data interjection features, this HIL testbed demonstrates a comprehensive solution for testing low-power devices and those requiring high inrush current, such as FPGAs. The modular design of the testbed allows for easy expansion and adaptation to meet the evolving needs of modern embedded systems. It serves as a foundation for future work to integrate this system fully into signal analysis software suites, which could further streamline the testing process and enhance data analysis capabilities.

The remainder of this report is organized as follows: Chapter 2 discusses the related work, providing background on previous research and developments of current measurement, HIL testing and industry devices. Chapter 3 delves into the fundamentals, explaining the concepts and principles necessary to understand the design and implementation of the testbed. In Chapter 4, each module's detailed design and implementation are described, highlighting their key features and performance aspects.

Chapters 5 and 6 focus on the processing system and programmable logic, as well as the simulation of the analogue circuit, which provide essential insights into the current measurements' performance and potential for optimisation. The experimental setup, including the methodology and equipment used in the testing process, is detailed in Chapter 7. Chapter 8 presents the results obtained from the experiments, demonstrating the capabilities and performance of the testbed.

An in-depth discussion of the findings and potential improvements is provided in Chapter 9, followed by a conclusion in Chapter 10 that summarises the key contributions of this work and highlights the potential of the testbed as a foundation for further development in hardware in the loop (HIL) testing for embedded devices.

Chapter 2

Related Work

In this chapter, an overview is presented of previous research in the areas of power profiling, power delivery, and sensor emulation. These three topics are of fundamental importance for designing, testing, and evaluating modern electronic systems, particularly in mobile computing and embedded systems.

Since the early days of electronics, it has been crucial to have reliable and reproducible testing environments to verify electronic device performance and functionality. Power profiling, power delivery, and sensor emulation are all essential tools that enable engineers to evaluate the behaviour and characteristics of electronic systems under different conditions.

The following sections review previous work in these areas, highlighting each approach's key contributions and limitations and starting with a discussion of power profiling in chapter 2.1, which involves measuring and analysing the power consumption of electronic systems. In section 2.2, a review of research on sensor emulation is shown, including techniques for simulating sensor output and testing and debugging sensor-based systems. Lastly a general overview of industry devices is given in chapter 2.3.

2.1. Power Profiling Methods

2.1.1. Dual shunt resistor stage

A characterisation of the automatic switch-over of shunts to create a higher dynamic range was given by Pötsch et al. [4], where the authors propose a measurement system for tracking the dynamic power consumption of wireless embedded systems. The system uses a dual shunt resistor stage with an automatic switch-over, which allows for a wide dynamic measurement range of 50 dB (1 μA to 100 mA) with an average measurement error of 1.2%. The system also employs two zero-drift current sense amplifiers and a 16-bit SAR ADC for each amplifier, resulting in a higher thermal noise performance and a higher total measurement resolution than a single shunt solution. The measurement system is connected via Ethernet and can forward power samples to a remote computer at a sampling rate of up to 250 kHz.

Using a dual shunt resistor stage and multiple current sense amplifiers allows for a high measurement resolution and low noise performance. The Ethernet connection enables the system to integrate into a remote monitoring setup easily. However, the authors stated that future work is needed to complete the signal processing and communication part. They furthered this work with [5] in the next chapter 2.1.2.

2.1.2. Highly dynamic power consumption measurement

For tracking the highly dynamic power consumption of wireless embedded systems commonly found in IoT devices, the authors of [5] presented a continuation of their previous work [4] on measurement solutions for highly dynamic currents. The system uses a dual shunt resistor stage (100 Ω and 1 Ω) with an automatic switch-over controlled by a Schmitt-trigger, dynamic measurement range from 1 μA to several hundreds of milliamps at a ADC resolution of 16 bits. No timing specifications were given on the switching speed. The system can evaluate the timing relation of proprietary RF communication and forecast the expected battery life of a Wifi-based data acquisition system. Above 100 mA both ADCs are in saturation, but the authors achieve coarse current measurement by measuring both the supply voltage and the effective load voltage. [5, p3, eq2]

2.1.3. Shunt Resistor in the loop

A method for estimating the power consumption of peripheral devices while focusing on low development costs in embedded microcontrollers is presented by the authors of Berthou et al. [6]. The method is demonstrated using MSP-EXP430FR5739 nonvolatile RAM and various peripherals on an MSP-EXP430 platform. This allows for measuring all individual peripherals, providing an often overlooked aspect in similar research. A simulator for any instruction set architecture, and peripheral is developed that allows for

adaptation. The simulator is designed for an MSP-EXP430 platform with an accelerometer, a temperature sensor, and an external radio chip. It achieves an accuracy of 1% in time and 5% in energy consumption estimation, which is more than two orders of magnitude worse than industrial solutions, but the focus was on low development cost.

The main contribution of this work is a simplified power model that enables the accurate simulation of ultra-low power embedded systems using peripherals. The simulation model runs the driver part symbolically by bypassing the whole routine and only simulating its functional effect. The simulator is particularly well-suited for intermittent systems simulation.

2.1.4. Hal Effect Current Sensing

The growing use of linear Hall-effect sensor ICs in open-loop current sensing and measurement applications is shown by Emerald [7]. These sensors offer non-intrusive, safe, and isolated detection of high current levels without dissipating significant power. The applications for these sensors are diverse and continue to expand as designers seek to protect systems, create more reliable equipment, and address safety issues. Current linear Hall-effect sensors have tolerances and temperature drifts that can pose challenges for those designing systems that require single-digit accuracy over a wide range of operating temperatures. The measured voltage from these devices is stated as ±10 G. At low currents, this can correspond to ±50% errors, but at higher currents, with a magnetic field of ≥667 G, drift is present in the same way, inducing a 1.5% error and indicating a nonlinear relation. This facilitates Hall effect measurements for high current applications. Though future linear sensors may allow for programming after packaging, enabling users to tune the gain, calibrate the output quiescent voltage, and compensate for temperature variations. The authors predict that the opportunities for applying these sensors will continue to expand and multiply as the need for power electronics systems evolves.

2.1.5. Mobile Power Logger for Prototyping IoT Devices

A fully realised hil testbed with a focus on current measurement is shown in Sigrist et al. [3]. In which the authors describe the RocketLogger, a mobile data logger. The RocketLogger combines two circuits, the shunt resistor-based circuit for higher current measurements (max 500 mA) and the feedback ammeter-based circuit for low current measurements (min 5 nA) for a combined range of 165 dB. The switching between these two stages occurs in 1.5 μs. It is intended for use in the testing and characterising of energy-harvesting IoT devices, particularly those with ultra-low sleep currents and high communication current requirements. The authors present the RocketLogger's capabilities through a sample energy harvesting application, including its fast and seamless auto-ranging and easy-to-use remote user interface.

2.2. Sensor Emulation and Injection

To thoroughly test a device under test, one needs to be able to simulate the DUT operating conditions and interaction with other devices. In a reproducible test setup, these would not be connected but simulated. This is where the field of sensor emulation and data injection is used.

2.2.1. Automation in HIL Units Development and Integration

The automation of the process of configuring and developing hardware in the loop (HIL) systems is proposed in Brayanov and Eichberger [8]. Their work is able to create and configure HIL simulations on the signal level, and their aim is to reduce the complexity, cost, and setup time required for HIL systems, by using low-cost hardware and a model-based approach for the generation of firmware for distributed HIL systems. The approach generates model based firmware for the HIL,

The authors suggest that this approach has the potential to make HIL systems cheaper, faster, and more widely used, which could lead to faster product development and safer products. However, it is also noted that the approach is limited to signal-level HIL simulation and would require additional formal specification of subsystems and specialized equipment to be applied on the power or mechanics level. Despite these limitations, the proposed approach is considered a good example of the application of formal development methods for the automation of the development process and shift left development."

2.3. Industry Devices

In the final section of this chapter, we will review a selection of commercial devices and tools that are available on the market for power profiling, power delivery, and sensor emulation. These tools are widely used in industry and can serve as helpful reference points for practitioners in these fields. By compiling them here in the table Industry Devices and contrasting these tools with the research approaches discussed in this chapter, we aim to provide a comprehensive overview of the current state of the industry in these areas.

Brand	Digilent	Dream Source Lab	Nordic	SALEAE
Device	Analog Discovery 2	DS Scope	Power Profiler Kit 2	Logic Pro 16

Inputs				
Multi-Use (A/D/Both)	2 + 16	2	2+8	16
Input Resistance	1MΩ	1MΩ	?	2 MΩ
Input Capacitance	16 pF	16 pF	?	10 pF
Input Protection	± 50 V	± 100 V	?	± 25 V

Digital				
Sample Rate (max)	100 MS/s	-	100 kS/s	500 MS/s
Supported Logic Levels	1.8 to 5 V	-	1.65 to 5.5 V	1.2 to 5.5 V
Able to stimulate data	Yes	-	No	No

Analog				
Sample Rate (max)	100 MS/s	1GSa/s	?	50 MS/s
Bandwidth (-3dB)	9 MHz	100 MHz	50 kHz	5 MHz
Max Current	-	-	1A	
ADC Number of bits	14 bits	8 bits	14 bits	12 bits
Min/Max Resolution bit	0.32 / 3.58 mV	0.31 / 62 mV	0.2 / 1000 μA	
Input Voltage Range	-25 to 25 V	± 100 V	0.8 to 5.0 V	-10 to 10 V

Power Supply				
Voltage Range	0.5 to 5.0 V	-	0.8 to 5.0 V	-
Rated Power	2.1 W x2	-	5 W	-

Physical				
Size	82 x 83 x 22 mm	115 x 74 x 16 mm	?	92 x 92 x 15 mm
Weight	?	?	?	220 g
PCB Layer	?	?	4	8
USB Type	USB 2	USB 3.0	USB 2	USB 3.0
Price	399 $	399 $	92.50 $	1399 $

Table 2.1.: Summary of related industry devices.

Chapter 3

Fundamentals

This chapter is meant as a refresher on the protocols and techniques used to develop the different modules and analogue circuitry.

3.1. Sensing Elements for Current Measurement

Fundamentally the analogue world can be translated to the digital domain with only a few basic parameters to be then analysed with computers. Current needs to be measured for many purposes and functionalities, with only one power usage specification. In literature, as seen in [4], [6], [7] or [3] three main ways of measuring current have crystallized. In the following subchapters, we will have a look at these variants.

3.1.1. Current measurement using Shunt Resistor

A shunt resistor is a low-impedance resistor used to measure a circuit's current flow. Low impedance stands in contrast to the impedance of the circuit the shunt is supposed to evaluate. It is connected in parallel with the load, and the voltage drop across it is measured using a voltmeter. The current flowing through the circuit can then be calculated using Ohm's Law, which states that the current through a conductor between two points is directly proportional to the voltage across those points and inversely proportional to the resistance between them. Shunt resistors are often used in high-precision current measurement applications because they have very low resistance $R_{Shunt} << R_{Circuit}$ and do not significantly affect the circuit in which they are placed. They can also be used with an amplifier and a display device, such as a digital multimeter or analog to digital converter (ADC), to allow for easy reading and analysis of the measured current.

Lastly, choosing the resistance of the shunt is a tradeoff between the accuracy of the later measurements and a low interference with the device under test (DUT)s circuit.

3.1.2. Measurement using Hall Effect sensor

A Hall-effect sensor is a non-intrusive and isolated detection of high current levels without dissipating significant power. It involves detecting the presence or magnitude of an electric current without interrupting the flow of that current. This is achieved by measuring the magnetic field generated by the current. By analysing the resulting voltage, the current can be determined. One downside of this technique is the interplay between different measurement lines in the same vicinity and the crosstalk seen on one measurement from the state of the other. A last drawback of this technique is the limitation that on high current applications, as seen in the calculations of [1] a 200 A current creates a 13.33 Gauss magnetic field at a distance of 3 cm. This gives an output voltage of 67 mV from the Hall effect sensor. Thus, there are more feasible alternatives for currents ranging in the uA or even nA.

3.1.3. Direct Current Resistance

A direct current resistance (DCR) circuit is a space-saving, lossless circuit shown in figure 3.1, which necessitates tuning for proper functioning since it uses the parasitic resistance of an inductor as the current load in contrast to an actual resistance like the shunt. This means further steps must be taken during manufacturing to guarantee the circuit works correctly. The reactive components have a wide range of tolerances which can cause considerable differences in the effective resistance between circuits. Inductors and capacitors have strong temperature dependencies, which can lead to circuit inaccuracies when tuned. The DCR circuit architecture is suitable for measuring gross currents at low supply voltages while maintaining a lossless structure with the lack of components in series with the regulator.

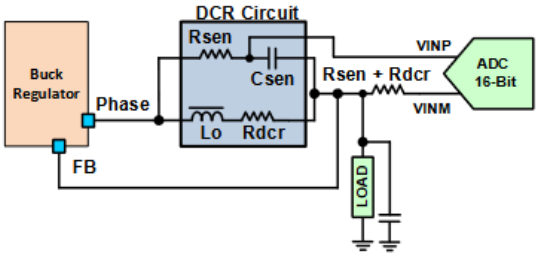


Figure 3.1.: Simple Schematic of a DRC Circuit from [1]

3.2. Hysteric Circuit

Hysteric amplification circuits are electronic circuits that use the phenomenon of hysteresis to output a signal from an OpAmp, depending on the history of the signal. Hysteresis is the property of a system to have a different response to an increasing versus a decreasing input, as visible in figure 3.3. In a hysteresis amplification circuit, the input signal is applied to a control element connected to a feedback loop, such as a transistor or a resistor. The output of the control element is then compared to a reference level with R_3 in schematic 3.2, and the result is used to adjust the gain of the amplifier. One advantage of hysteresis amplification circuits is that they can provide a high degree of linearity and stability over a wide range of input signals. This makes them useful for applications requiring precise amplification and control, such as instrumentation and control systems. Another advantage is that hysteresis amplification circuits can be easily implemented using various technologies, including analogue and digital circuits. This allows them to be used in many applications, from simple signal processing to complex control systems. However, there are also some limitations to hysteresis amplification circuits. One potential drawback is that they require a relatively large amount of power to operate since one connects a supply rail with two resistors to the ground plane while wanting to keep their impedance low enough to create a smaller RC constant and faster-switching characteristics. This limits their usefulness in portable or battery-powered systems. Additionally, they may be more complex and challenging to design than other types of amplification circuits, with the output being routed back into one input, thus being prone to oscillations.

As per Texas Instruments [9] to calculate the necessary components for the comparator with hysteresis, one should first select the switching thresholds for V_{Sense} for when the comparator will transition from low to high (V_L) and high to low (V_H) visible in figure 3.3. Also, using a sufficiently large $R_1 \pm 100kOhm$ to minimise the current draw is recommended, although care must be taken not to create too big of a low pass filter. Then the final two resistances become:

$$R_2 = \frac{V_L}{V_{CC} - V_H} \cdot R_1 \tag{3.1}$$

$$R_3 = \frac{V_L}{V_H - V_L} \cdot R_1 \tag{3.2}$$

All of these together create the hysteresis width of $V_H - V_L$ with all resistances having a t_{RX} tolerance.

By refactoring this into equation 3.3, one can infer that the tolerances t_1 and t_2 are directly linked to the size of the hysteresis width while t_3 is inversely linked.

$$V_H - V_L = \frac{1}{1 + \frac{t_3 \cdot R_3}{t_1 \cdot R_1} + \frac{t_3 \cdot R_3}{t_2 \cdot R_2}} \cdot V_{CC} \tag{3.3}$$

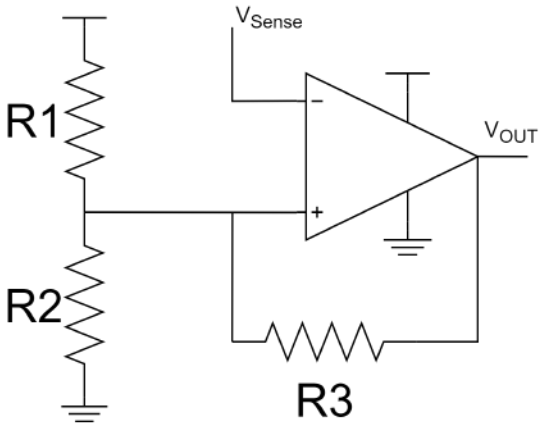


Figure 3.2.: Hysteric Circuit

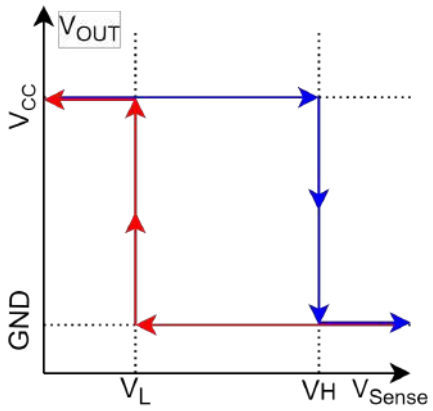


Figure 3.3.: Voltag Plot for Hysteric Circuit

3.3. ADC Precision and Resolution

Analog to digital converter (ADC) convert continuous analogue signals into discrete digital ones. The resolution of an ADC is the tiniest change in analogue voltage that can be detected and converted into a digital value.

The resolution of an ADC is determined by several factors, including the number of bits used in the converter, the reference signal that the input gets compared to, the amplitude of the input signal, and the noise level in the system. A higher number of bits generally leads to better resolution as smaller voltage steps can be measured, increasing the possible digital output values. These possible values get compared to an independent reference voltage.

One way to improve the resolution of an ADC is to use a successive approximation technique by setting a threshold voltage compared to the analogue input signal to determine the digital output value. The threshold is then adjusted based on the result of this comparison, and the process is repeated until the desired resolution is achieved.

Another way to improve ADC resolution is to use oversampling techniques. This involves sampling the input signal at a higher rate than the desired sampling rate. This allows for

averaging over the signals received during one sample period, which reduces noise and gives a more accurate representation of the signal, increasing its resolution.

Finally, ADC resolution can be improved using signal conditioning techniques such as filtering and gain adjustments. These techniques reduce noise and improve the signal-to-noise ratio, thus improving resolution.

The calculation of the actual resolution of an N-bit ADC is

$$Resolution\ \ per\ \ bit = \frac{Amplitude}{2^N} \tag{3.4}$$

3.3.1. Noise in Measurements

Noise in signal lines is a common problem encountered in the context of ADC measurements. Minimising the noise in the measurement line is critical to measure and recording analogue signals accurately.

One common noise source in signal lines is electromagnetic interference (EMI), which can arise from various sources such as other electrical equipment, power supplies, or nearby radio frequency transmitters. EMI can cause unwanted fluctuations in the signal line, leading to inaccurate ADC readings. Another source of noise is thermal noise, which is typically proportional to the square root of the temperature and can therefore be minimised by cooling the measurement equipment or calibrated out by applying a thermal measurement device on

In addition to these noise sources, other factors, such as ground loops where multiple paths to the ground are present for a circuit, resulting in unwanted currents flowing through the measurement circuit, stray capacitances, and switching noise, can also contribute to measurement line noise.

To mitigate these sources of noise, various techniques can be used. Shielding the signal line with a grounded conductive layer can help reduce EMI, while minimising the length of the signal line can reduce its susceptibility to other noise sources. Adding bypass capacitors to the circuit can also help to filter out unwanted noise. Lastly, choosing power delivery components like LDOs instead of bucks reduces the variance in the power supply of the measurement components like the InAmp, drivers or ADCs, since the LDOs output a more stable and noise-free power rail.

3.3.2. Effective number of bits

The effectiveness of an ADC can be measured by its effective number of bits (ENOB). It is defined as the number of bits necessary to achieve a given signal to noise and distortion (SINAD). ENOB is used to quantify the resolution and accuracy of a given ADC, as well as its dynamic range and linearity. The definition most used in literature is [10] equation 1 here eq. 3.5.

$$ENOB = \frac{SINAD - 1.76dB}{6.02} \tag{3.5}$$

To give an example of this with the AD7134 ADC, we use in this project. The ADC is 24-bit and has a SINAD of 106.5 dB in its high-power sampling mode per the datasheet [11]. This would then calculate per eq. 3.5 to a ENOB of 17.4 bits that starkly contrasts with the expected 24 bits. Thus over the entire 4.1 V amplitude that is the reference voltage to the ADC, we only calculated an achievable resolution of 23.7 μV per bit step instead of the originally expected 0.24 μV per bit when one contrasts the 17.4 bits versus the initially expected 24 bits.

Chapter 4

Design Implementation Of Modules

In this chapter, we dive into implementing and designing the crucial modules responsible for creating this hardware in the loop (HIL) test environment. The chapter covers the design and implementation details of the power profiler module (PPM), power delivery module (PDM) and data interposer module (DIM) designed for this thesis and additionally the FPGA SoC Module integrated into this work. A particular emphasis will be given to addressing the most significant challenge faced in the power profiler module: the hysteric cascade that drives the shunt resistor for dynamic range current measurement and the corresponding high power mode that pauses this cascade.

4.1. Modularity

We employ a PCIe X1 connector from the compute board to the different modules to guarantee modularity and the ability to support future modules. For this proof of concept, we only have one connector per module. Still, the choice of FPGA and power delivery is designed to sustain multiple measurement, delivery and interposer modules for future versions, with the FPGA's ability to reroute all I/Os to accommodate not yet designed functions and modules.

4.2. Power Profiler Module

The power profiler module (PPM) represents the novel work of this thesis. As visible in the block diagram, the PPM 4.1 employs a combination of hysteresis circuits chained (cascaded) together to control the shunt resistance used for current measurements. A novel way of combining this low current measurement is implemented with another kelvin-connected shunt for higher currents. Its hysteresis circuit can halt the

low current cascaded circuits and short the shunts not to increase voltage drop over the measurement circuit. Additionally, two voltage measurement terminals are implemented. These four terminals output the voltage into a driver /ADC combination for four data channels. An EEPROM is on the module to store module identification and calibration data.

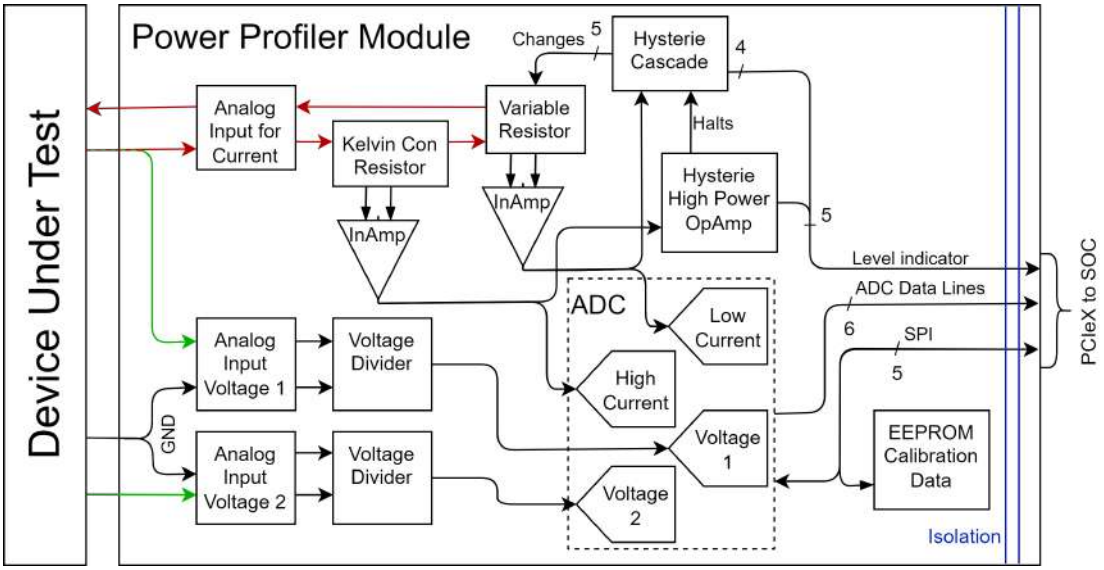


Figure 4.1.: High Level Block diagram of PPM Data and Measurement Lines

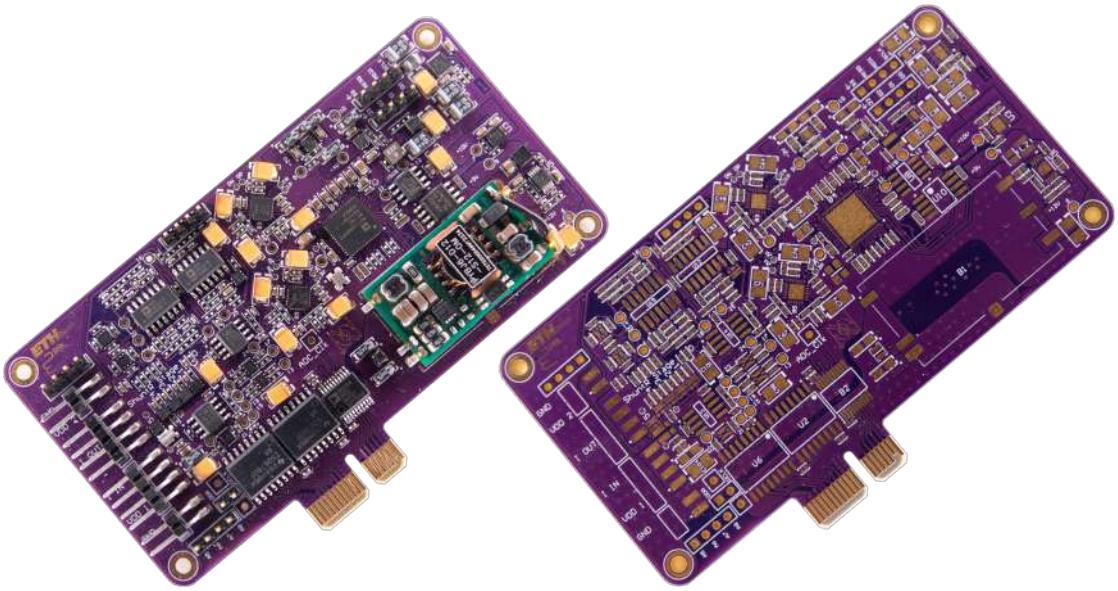


Figure 4.2.: Power Profiler Module

4.2.1. ADC AD7134

The AD7134 [11] is a quad-channel analog to digital converter (ADC) offering high-density multi-channel data acquisition in a small form factor. The ADC has an integrated asynchronous sample rate converter that supports a wide range of output data rates and digital filter profiles, including options for frequency domain analysis, low latency time domain analysis, and optimal noise performance. The ADC also supports on-board averaging for improved dynamic range and offers two device configuration schemes, SPI and pin control mode. With our implementation, the system uses a 5V source voltage and has a 4.096V reference voltage with a common mode voltage of 2.048V. It employs four separate ADC converters that aren't interconnected, and the data is output on six serialisation lines to the FPGA. The ADC runs with a CMOS-given clock of 48 MHz and can output 1.5 MS/s in low power mode and 374 kS/s in high performance mode we use. In appendix A.2 table A.1 are all SPI reprogrammed registers that differ from the reset values.

This analog to digital converter was chosen since it has a high 107.21 dB dynamic range and RMS Noise of 12.μV at 374 kS/s and four different measurement channels.

4.2.2. Instrumentation Amplyfier

We employed the AD8421ARZ, an instrumentation amplifier from Analog Devices [12] to amplify the voltage drop over the shunt resistor. Its high CMRR of 120 dB allows for an accurate and steady amplification, even when the input signals vary over time. Its low offset voltage of 60 μV minimises drift and temperature-related errors. Furthermore, the amplifier has a low input bias current of 500 pA.

Due to other constraints in the system, the amplifier will receive a maximum voltage of 50 mV. Therefore, to measure in the full amplitude range of the ADC at 4.1V, an amplification of $4.1V \div 0.05V = 82$ is necessary, which is achieved with an external resistor of 122 Ohm. At this amplification, the settling time to 0.0001% is 0.5 μs and the bandwidth three MHz and thus not a significant source of error compared to the MOSFET slew time or the ADC sampling rate.

To sample the entire voltage range of 0.8V to 5.5V, a positive supply of 10V and negative rail of -4V was desired, finally leading to the diamond plot in figure 4.3 of our instrumentation amplifier.

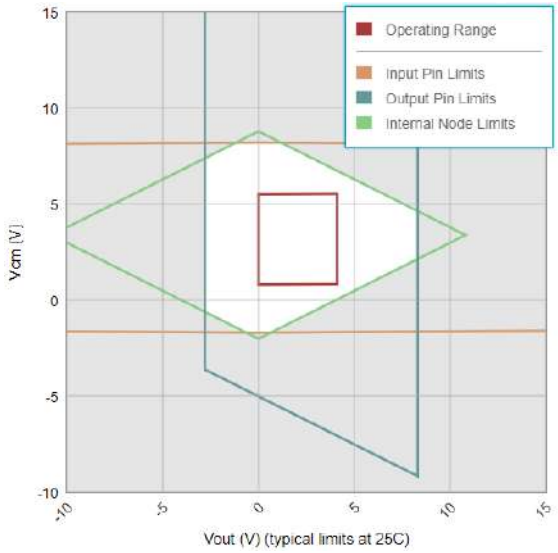


Figure 4.3.: Diamond Plot of AD8421ARZ under design specifications

4.2.3. Driver Input to ADC

The accuracy and precision of the ADC rely heavily on the proper biasing of the input voltage. The ADA4940, a high-performance operational amplifier, is designed to provide the necessary drive to precisely push both positive and negative input voltages to the ADC. The driver is operated in inverting mode with 2V/V gain to transform the 4.1 V input into ± 4.1V. The absolute maximum performance of the AD7134 is set at 374kSps in high performance, and with the other settings mentioned in chapter 4.2.1, we thus get a maximum input frequency that is allowed at 1/2 of this at 187 kHz. At these frequencies of the ADC and driver system, the noise and distortion values can be seen in table 4.4 and the contribution of the system total harmonic distortion (THD) over all frequencies can be seen in figure 4.5

Noise and Distortion at 187 kHz	
Parameter	**Value**
THD	-139 dB
ENOB	17.3 bits
SINAD	106 dB
SNR	106 dB
System Noise	14.6 uVrms

Figure 4.4.: N&D Summary

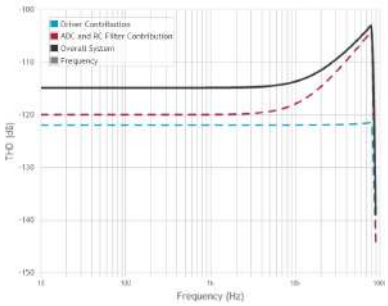


Figure 4.5.: Contributions to System THD

4.2.4. Variable Shunt Resistor

Using a shunt resistor is inherently limited by the resistance R_S that one can reliably create with the presence of trace resistances and other components in the circuit. The MOSFETs we use to engage the variable shunt resistor are by design inside of the circuit sector that the voltage drop is measured from as visible in figure 4.6, and thus their drain to source resistance R_SD needs to be accounted for. R_SD is highly temperature dependent and at room temperature the MOSFETs we use already have a R_SD of ($11 \pm 4)m\Omega$.

Thus $R_S >> R_SD + R_{Trace}$ for this setup to reliably create the expected voltage drop. The shunt resistances in total for our design are limited to equal about 50 $m\Omega$ to anticipate the created voltage drop still correctly. This number can be determined by looking at the inherent resistance R_SD of the MOSFETs and their temperature-dependent variability. With the error propagation equation 7.1, one can arrive at $61 \pm 4.03 m\Omega$ resistance, which is already a 6% variability. For this prototype, we decided on one magnitude step per resistor. Find the desired resistance values and the corresponding resistances that are needed to create this parallel resistance in table 4.1 with the resulting current ceiling if the desired voltage drop of 50 mV is to be maintained.

Desired Resistance	Installed R	Current ⇑	Current ⇓
1000 Ω	1000Ω ±1%	50 μA	-
100 Ω	111Ω ±1%	500 μA	378 μA
10 Ω	11Ω ±1%	5.046 mA	3.783 mA
1 Ω	1Ω ±1%	55.046 mA	38.147 mA
50 $m\Omega$	$51m\Omega$ ±1%	1.035 A	342.511 mA
$5m\Omega$	$m\Omega$ ±1%	-	342.511 mA

Table 4.1.: Variable Shunt Resistor Resistances

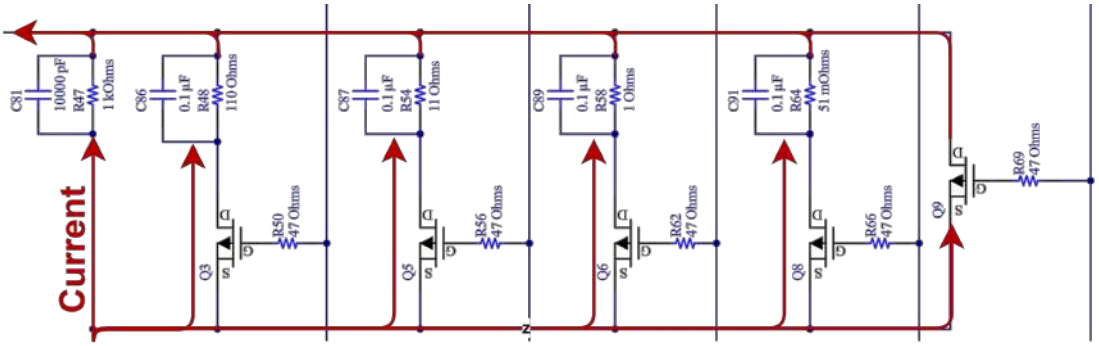


Figure 4.6.: Variable Shunt Resistance Schematic

4.2.5. Hysteresis Cascade

To engage these variable shunt resistors, we employ multiple hysteric opamps in series that use the instrumentation amplifier as input V_{Sense} (TPH18), as visible in figure 4.7. This has the voltage drop over the shunt as input, so care must be taken not to create oscillations. On the other hand, this creates a fast analogue circuit only majorly constrained by the RC low pass filter created by the InAmp. At InAmp state 0 V, all outputs 1,7,8 and 14 are high of the OpAmps and thus, only U12D has a + input of about 2 V because of the voltage divider made up of R_{41} and R_{42} while the other three are at 10 V. Thus U12D is the first to react to a change over V_H from V_{Sense}. Output 14 falls to the negative supply rail of -4 V, and with that, U12C from switch two is primed with the voltage divider. A state change can happen if V_{Sense} falls below V_L of U12D or rises above V_H of U12C. These state changes are accompanied by changes in the shunt resistance and V_{Sense}.

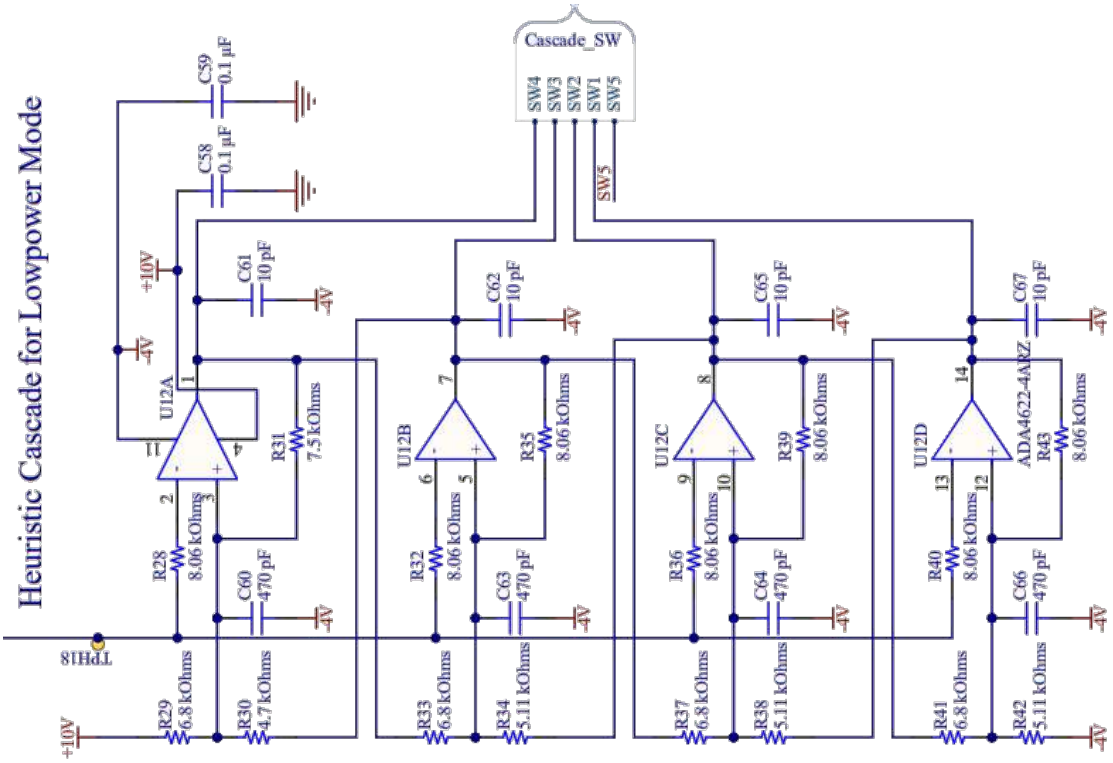


Figure 4.7.: Hysteresis Cascade Circuit Schematic

In chapter 3.2, we introduced equations 3.1 and 3.2 for the calculation of the resistances in one hysteric circuit. Now we want to dimension the falling Voltage V_L of the circuit in comparison to the rising Voltage V_H of the previous circuit. We introduce an arbitrary tolerance $1-t$ of 2% to the voltage level to minimise oscillation. The following calculations

are dependent on the in stage X currently engaged shunt resistor R_{SX}, V_{HX}, V_{LX+1} and the corresponding tolerances T_C of the real world components used. We used 1% tolerance components for all resistances and the worst-case tolerance for the calculations. Using the worst case lets us dimension the hysteresis steps in a way that even with the most disadvantageous distribution, we do not create unnecessary oscillations. Equal in both scenarios are the currents I_X and $t \cdot I_{X+1}$ flowing in both stages with the difference of the introduced tolerance t. After the usual conversions, we end with equation 4.3 that allows us to dimension the falling Voltage V_L for each stage.

$$I_X = t \cdot I_{X+1} \tag{4.1}$$

$$\frac{V_{LX+1}}{T_{R_{SX+1}} \cdot R_{SX+1}} = t \cdot \frac{V_{HX}}{T_{R_{SX}} \cdot R_{SX}} \tag{4.2}$$

$$V_{LX+1} = t \cdot \frac{T_{R_{SX+1}}}{T_{R_{SX}}} \cdot V_{HX} \cdot \frac{R_{SX+1}}{R_{SX}} \tag{4.3}$$

With these calculations, the maximum ADC voltage range of 4.096 V that is defined as the V_H of the hysteresis, a R_1 chosen to be 6.8 kOhm and the desired shunt resistances determined in chapter 4.2.4, we can now determine the ideal makeup of the hysteric amplification cascade. As discussed in chapter 3.2 with the worst-case swing of the tolerances and resistances available on the market, the final makeup of the cascade looks as seen in table 4.8. These calculations have been programmed in a helper script **cascade_helper.ipynb** in the **Spice** project repository.

Stage	V_L	tol	$V_H - V_L$	ideal R_2	ideal R_3	final R_2	final R_3	tol
1	0.401 V	± 1.48 %	3.695 V	5068 Ω	8099 Ω	5100 Ω	8060 Ω	± 1 %
2	0.398 V	± 1.48 %	3.698 V	5065 Ω	8087 Ω	5100 Ω	8060 Ω	± 1 %
3	0.368 V	± 1.48 %	3.728 V	5030 Ω	7966 Ω	5100 Ω	8060 Ω	± 1 %
4	0.212 V	± 1.48 %	3.884 V	4851 Ω	7374 Ω	4700 Ω	7500 Ω	± 1 %

Figure 4.8.: Cascade Components

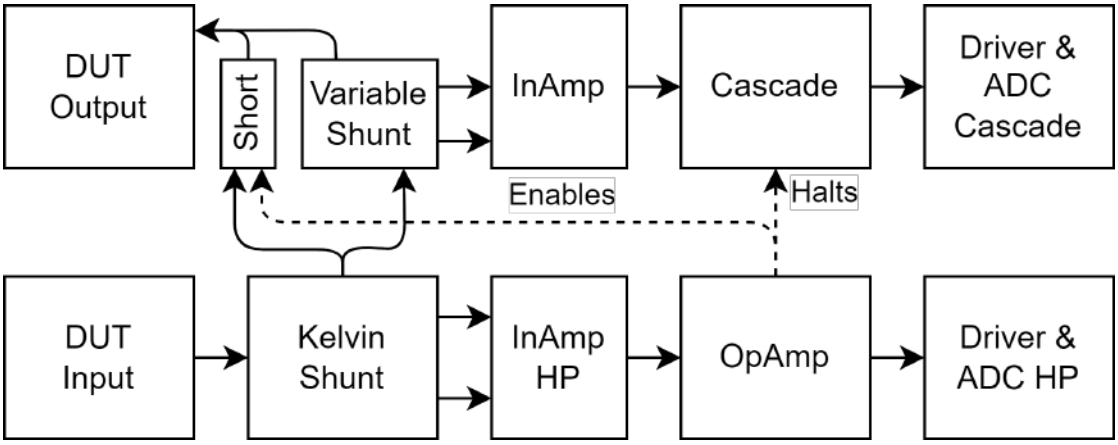


Figure 4.9.: High Power Mode for Current Measurement

4.2.6. High Power Mode for Current Measurement

As described in chapter 4.2.4 the intrinsic resistance variability of the MOSFETs necessitates a workaround if one wants to measure higher currents while still keeping the variable shunt resistor design approach. We approached this in a novel way. We connected a small kelvin-connected shunt resistance in series to the variable shunt resistances. This shunt resistance is visible in figure 4.9. We need a secondary dedicated instrumentation amplifier (InAmp) and ADC to capture the resulting voltage. However, this approach is instrumental because it removes the MOSFET from the calculation altogether. As a result, we can easily measure a far more extensive current range without compromising on the high resolution of the lower currents. To avoid influencing the DUT circuit with a higher voltage drop than intended, removing the variable shunt from the testing circuit is necessary. We designed this functionality by having a parallel trace to the shunt that can be shortened with another MOSFET. This, though, would let the V_{Sense} fall to zero and with it, the cascade steps to the lowest level. So after disengaging the high power mode, the whole cascade would need to stabilise again, increasing the unusable data window from one step switch to four. Thus the also hysteric opamp of the HP mode enables a steady 4V source to the cascade input V_{Sense} to halt the cascade at switch four.

4.2.7. Power Planes

While multiple power planes are necessary for the module's functionality, a highlight needs to be set on the planes that supply the hysteric cascade, instrumentation amplifier and ADC since these need to be as removed from noise as possible. For this purpose, the general path was to convert the 12 V input from the isolator to the corresponding power planes with buck converters while introducing a Low-dropout regulator (LDO) before the measurement devices that clean the rail from any introduced noise from the supply or

buck. This intermediate step is necessary since, for example, when one would only use a LDO to convert a 12 V rail down to a 1.8 V rail with 200 mA of load current, this would create 2.18W of power dissipation on the area of a small coin or roughly equivalent to the heating output of a typical electronic stovetop scaled for the same area.

Plane	Current Density	Supply Target	Supplies
10 V	56 mA	100 mA	Cascade, OpAmp
5 V	62 mA	100 mA	Driver, Isolation, EEPROM
4.096 V	-	-	ADC
1.8 V	200 mA	300 mA	ADC, Isolation
GND	-	-	ALL
-2 V	-	-	Driver
-4 V	-	-	Cascade, OpAmp
-5 V	-	-	-2 V,-4 V LDO

Table 4.2.: Current Density on PPM

4.2.8. Isolation

Isolation is very important on a measurement device to mitigate power supply noise interfering with the measurements and also to keep any components safe from any electro static discharge (ESD) that might occur in either direction. Multiple isolation components are necessary to deliver power and send independent data over an isolation barrier. For generic data signals, we employ the ISO6760 [13] for high-speed independent data, and for timing critical data like SPI, we use the ADUM3150 [14] isolator specifically designed for the protocol and 4 secondary devices addressable by one secondary select line with an additional two-wire mux.

Since we filter the power planes again after the isolation, the power isolator didn't need to be measurement grade and needed to have enough throughput. Thus we went with the PYBJ6 [15].

4.3. Power Delivery Module

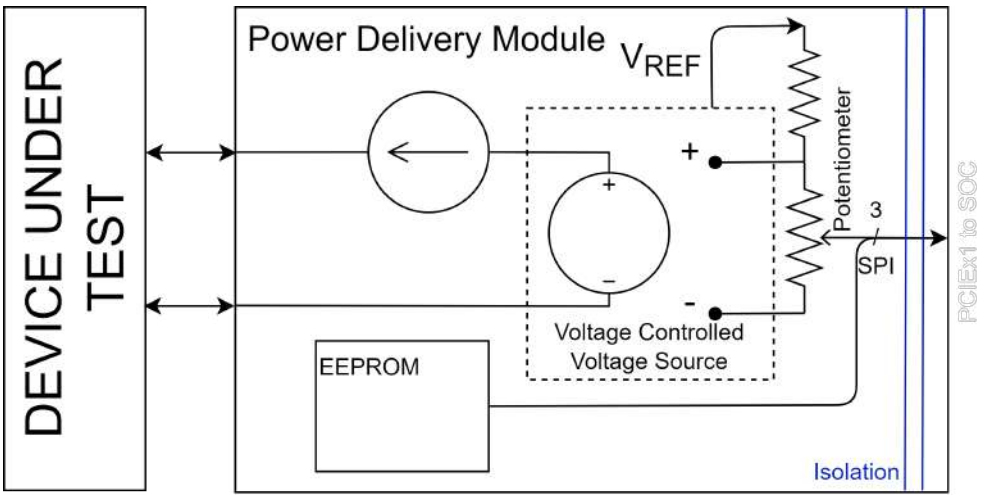


Figure 4.10.: Block Diagram of PDM

The power delivery module (PDM) represents a necessary step in sustaining a device under test environment even though it is not the driving focus of this thesis. The ability to sustain the most common power needs that a DUT in the embedded system world could have guided the design of this module. We can accommodate the range of 0.86 to 5.5 V with a max of 20 W or 10 A.

4.3.1. DC-DC Power Delivery to DUT

For the power delivery to a DUT, we employed the ATA010 by GE that could variably deliver the power needs, but without incorporating a current limiter which was left for future implementations. This module output voltage is set with an external resistance that can be changed at runtime. Thus the potentiometer AD5270 was introduced to the module, which entails 100 $k\Omega$ over a variability of 1024 settings creating a high accuracy desired output voltages. Only the range between 0.75 V and 0.86 V can not be set in this implementation since the resistance can not be set high enough to program the output to lower than 0.86 V. The test results for this setup are visible in chapter 8.5.

4.3.2. Isolation

Although the same isolators were used for data transfer as described in chapter 4.2.8, the power delivery modules required additional filtering to ensure (electromagnetic compatibility (EMC)) due to the high amount of power they could draw. This entailed a fuse and sufficiently large inductance coil visible in figure 4.11, which is also why the power delivery system for the module makes up over half of the area. Lastly, sufficient power delivery needed to be guaranteed so that the DUT could deliver up to at least 20 W of power as per the initial requirements definition of this system. Thus we installed a 30 W DC/DC isolator [16] to power the rest of the module sufficiently.

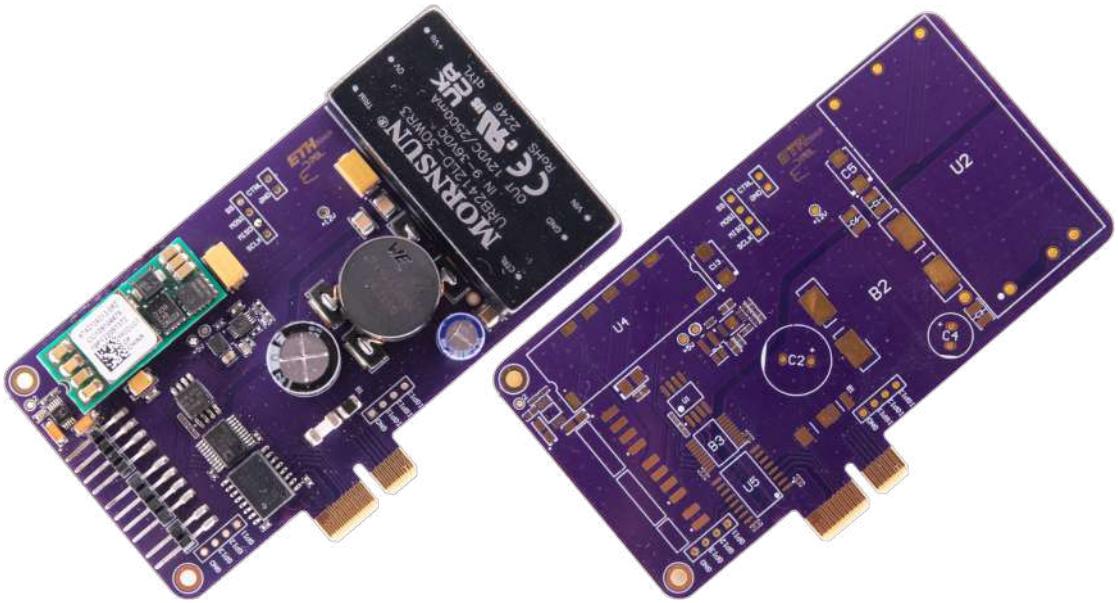


Figure 4.11.: High-Level Block Diagram of PDM Data and Power Delivery Lines

4.4. Data Interposer Module

At the initial stages of this thesis, a third module was planned. Still, after further feature definition, the use for version one of this module was only targeted at being able to interact with the DUT over an SPI bus as shown in figure 4.12. Thus this module was incorporated into the interposer board that connects FPGA SoC with the initial power plug and the different modules. The same SPI isolator was used to create this feature to get the necessary isolation of the DUT. Though with the shortcoming that the DUT needs to deliver the power to the isolator itself. This furthers the strain on the DUT with an additional 13.5 mA at peak frequency, but we deemed it acceptable for the first proof of concept before developing a dedicated module. The main can interact with up to four second devices on a single SPI line up to a data rate of 34 Mb/s.

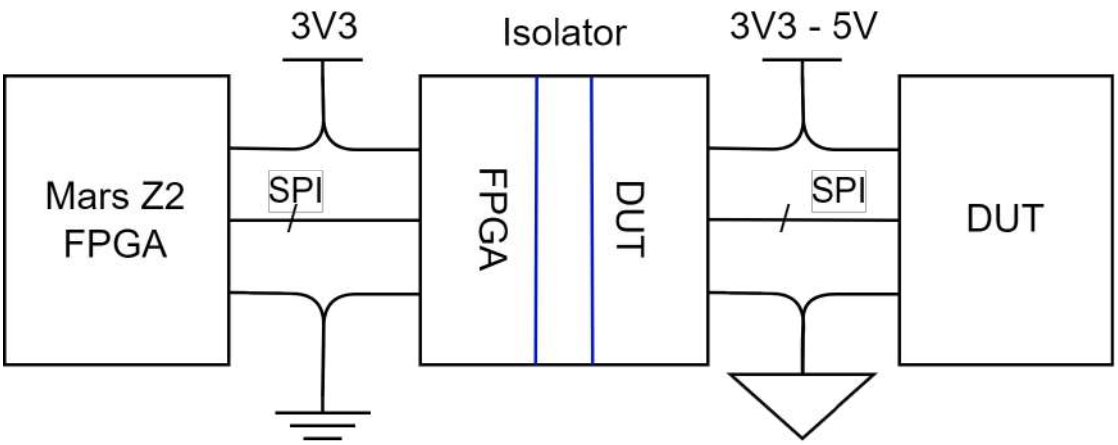


Figure 4.12.: Measurement Setup data exchange with DUT

4.5. Mars ZX2 Module

For running the prototype's firmware and real-time operating system, we used the Mars ZX2 SoC module by Enclustra. The Mars ZX2 System-on-Chip (SoC) module is an embedded processing system that utilises the Xilinx Zynq-7010 All Programmable SoC device. The module incorporates fast DDR3L SDRAM, quad SPI flash, a Gigabit Ethernet PHY, USB 2.0 On-The-Go PHY, and a real-time clock. It also contains an ARM chip and a field programmable gate array (FPGA) that allows for flexible development and high-performance data processing.

This module is designed in a small SO-DIMM form factor, which allows for space-saving hardware designs and easy integration into the target application, thus sing the Mars ZX2 SoC module can greatly reduce development effort and redesign risk when compared to building a custom SoC hardware.

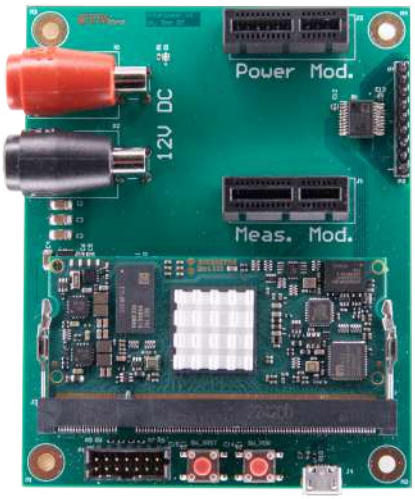


Figure 4.13.: Data Interposer Module

Chapter 5

Processing System and Programmable Logic

Separating the processing system (PS) and programmable logic (PL) allows for offloading specific processing tasks to the programmable logic, which can be optimised for specific operations. This can increase the system's overall performance and make it more efficient with the possibility also to implement advanced features and functions, such as parallel processing and hardware acceleration, which can further enhance the system's capabilities. As visible in figure 5.1, the data stream from the ADC gets handled by a register transfer level (RTL) module in PL that handles the data packaging further discussed in chapter 5.1. Still in PL is a FIFO for data buffering between clock domains and a direct memory access (DMA) module to save the data to the PS memory without halting the processing core operations.

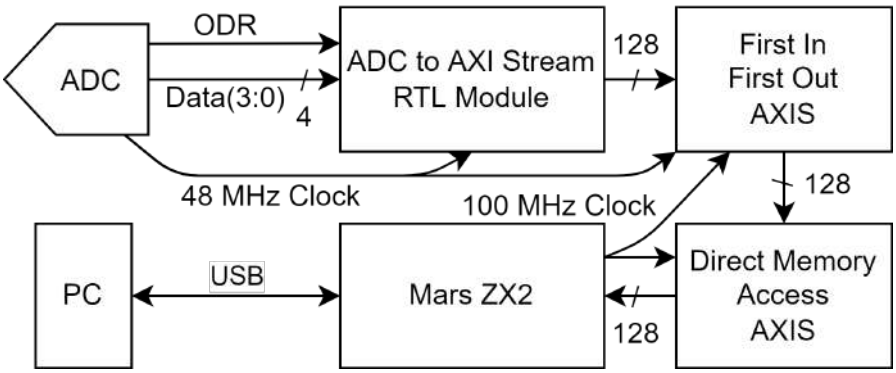


Figure 5.1.: Real Time Datastream from ADC to PC

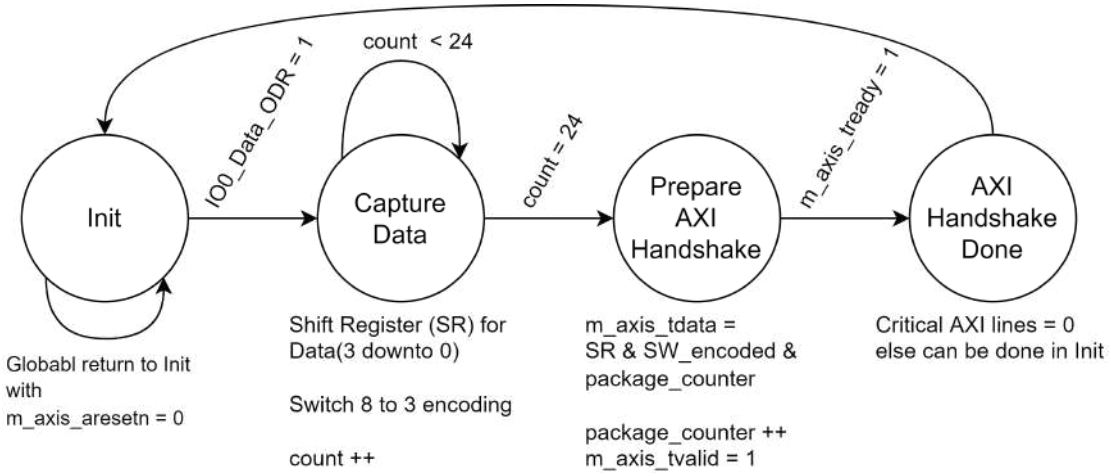


Figure 5.2.: State Machine of ADC RTL Module

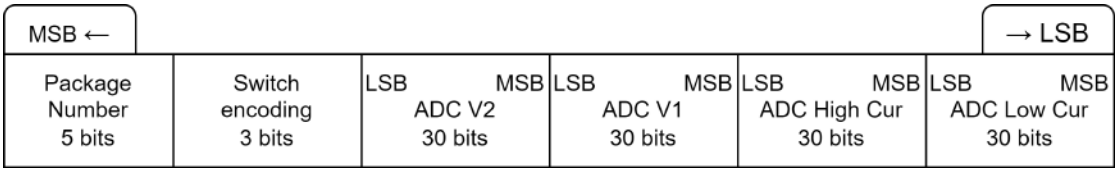


Figure 5.3.: 128-bit AXI Stream Package

5.1. ADC RTL Architecture

To better streamline the data gathering process that arrives from the ADC and be able to implement the data stream into existing programmable logic (PL) protocols, we wrote a register transfer level (RTL) module that takes the ADC clock, output data rate (ODR) and four data lines with the cascade switch signals and combines them to one 128 bit encoded package visible in figure 5.3. Figure 5.2 shows the state machine of this module.

Of note for this model is the AXI Stream, the standard interface to exchange data for Xilinx intellectual property (IP)s. This protocol employs a main and second relationship between two participating IPs with a valid and ready signal for a handshake. This behaviour was also implemented into the state machine, and these AXIS signals are visible with the designation m_axis since the module takes the role of main for the exchange.

Chapter 6

Simulation of Analog Circuit

As seen in chapter 4, the whole measurement setup is composed of a variable shunt resistor that is engaged by a hysteric amplification cascade and a high power mode to engage an additional in-series Shunt. The goal of this chapter is the comprehensive simulation and analysis of the critical analogue circuitry for the power profiler module (PPM).

6.1. Simulation Software

The simulations were done with advanced design systems (ADS) from Keysight, a software platform for electronic design automation (EDA). It provides a comprehensive suite of tools for designing and simulating radio frequency (RF), microwave, and high-speed digital circuits. ADS offers a range of features, including schematic capture, simulation, and layout, to help streamline the design process.

6.2. Simulation Settings

The simulation was done with a full recreation on the significant analogue circuitry of the power profiler module (PPM) and the official spice models for components like the instrumentation amplifier, the MOSFETs or, for instance, with the OpAmp the corresponding values were extracted from the datasheet. With these simulations, some possible changes in components to the implemented prototype will be highlighted and touched upon in the discussion chapter 9 to put some focus on design challenges and tradeoffs. The simulations which do not correspond to the current PPM version will be marked in the title with $\simeq$. Figures 6.1 and 6.2 correspond to a rising or falling current and to the step measurement that was flowing through the shunt resistance.

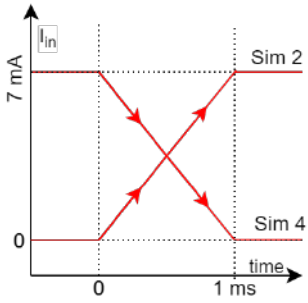


Figure 6.1.: Rising and Falling Currents

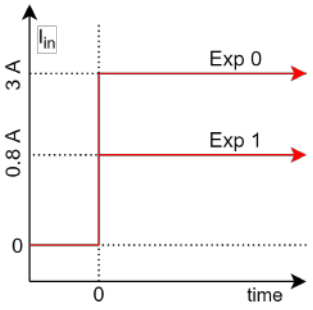
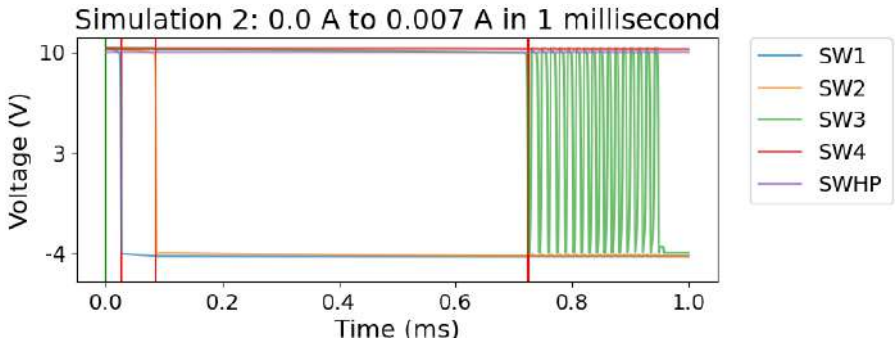


Figure 6.2.: Step Function Currents

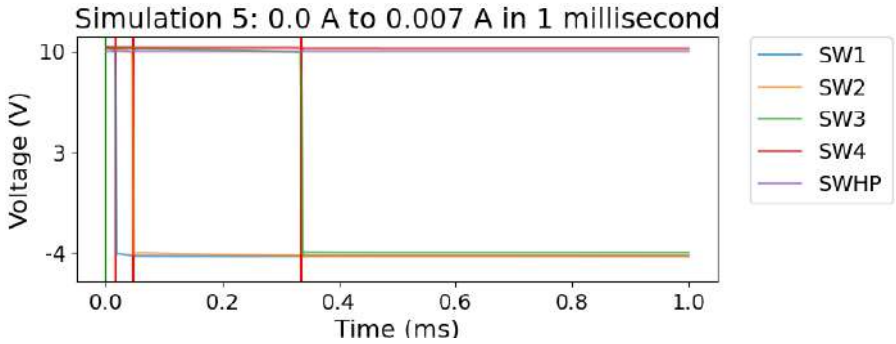
6.2.1. Rising Current 0A to 7 mA

In the zero to 7 mA operating range, one can see some oscillations in the state transition when switch three engages. Chapter 6.2.2 explores another design approach to diminish these oscillations. This behaviour will be further explored in chapter9.1, and the measurement setup is further discussed in chapter 7.2.



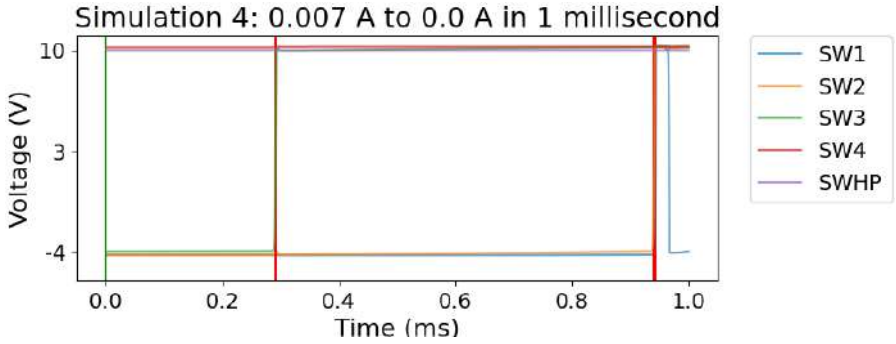
6.2.2. Rising Current 0A to 7 mA ≃ Bigger Resistor at MOSFET Gate

With the choice of one single MOSFET type for every current field comes a tradeoff. For smaller currents, these MOSFETs have too prominent of channel width and are thus switching slower, which creates an oscillation in the lower current fields. This could be improved or even remedied with an increase in the in-series resistance to the MOSFET gates, creating a more significant RC time constant that slows the switching behaviour. This behaviour is simulated here by increasing this resistance by one magnitude.



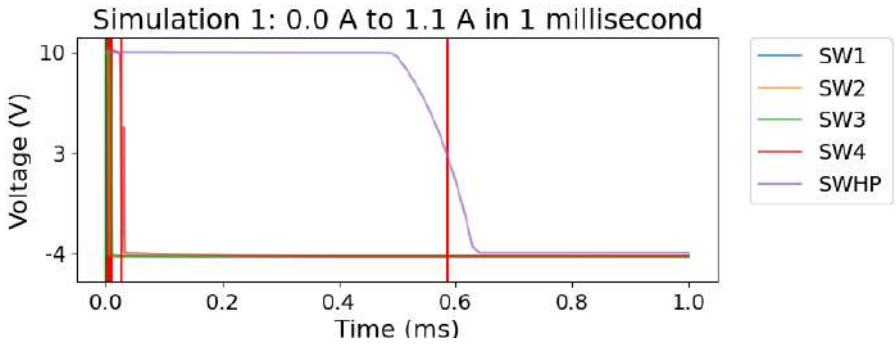
6.2.3. Falling 7mA to 0A

In the reversed current trend direction, these oscillations are not visible, yet an overcorrection of switch one is visible when switch two rose to a voltage high level.



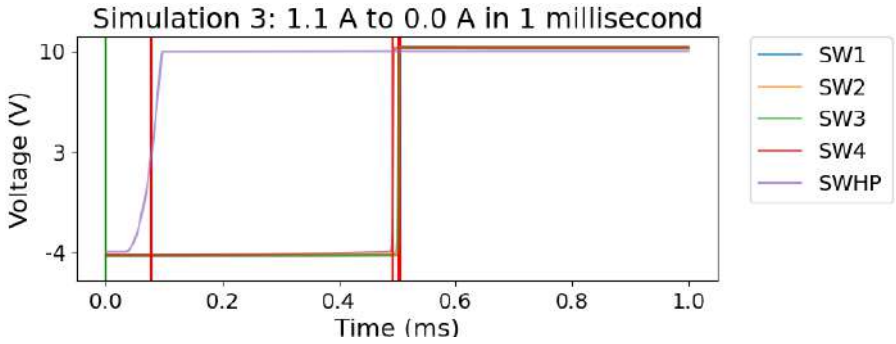
6.2.4. Rising Current 0A to 1.1A

For higher currents, this behaviour is not visible. On the other hand, the high power mode switch engages quite slowly in 0.1 ms compared to the expected μs switching range of the MOSFET. This behaviour could not be replicated in the prototype, and the device switches as expected, as seen in chapter 8.2.



6.2.5. Falling Current 1.1A to 0A

The reverse trend simulation shows the same slow rise time of the high-power switch five. No further oscillations take place.



6.2.6. Switching time of Cascade Steps

To simulate how fast the cascade can switch, a step function current was applied to the shunt resistance with a rise time of 1 ns. The step function of simulation experiment one was enough to trigger the high-power mode. In figure 6.3, one can thus see the high power mode engage almost instantly and halting the cascade in its current state with an engaging time of 1.7 μs.
When only enough current was applied to fully traverse the low-power mode as seen in figure 6.4, the cascade took 11.6 μs for all four stages, thus switching each step in 2.9 μs.

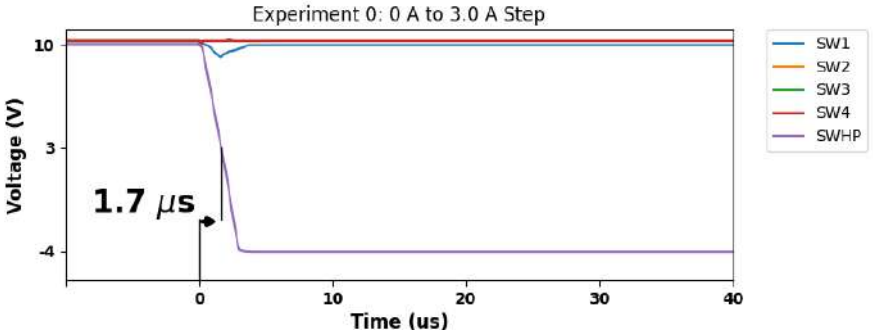


Figure 6.3.: Step Current Through Shunt at 3 A

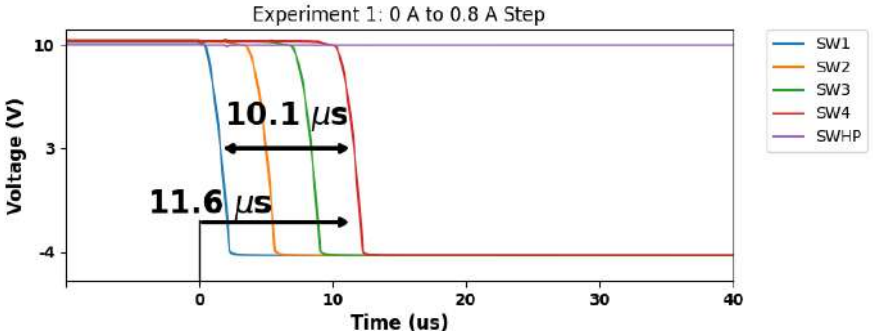


Figure 6.4.: Step Current Through Shunt at 800 mA

Chapter 7

Experimental Setup

In this chapter, the setup of all experiments is introduced with the definition of the ground truth corresponding voltage and current levels. If a file in this chapter is named and not explicitly told otherwise, one can find it in the enclosed git in the appendix D.

7.1. Definition Of Ground Truth

To create a reproducible and synchronizable ground truth, we employ the N6705 DC power analyzer by Keysight. This device can, on four different outputs in free or coupled mode, manage voltage up to 6 V and current load up to 3 A with variable slew and timing. For the experiments pertaining to the cascade, 3 A suffices to trigger all cascade steps and activate the high-power mode. One of the outputs can thus be set to send an arbitrary pulse coupled with the beginning of the current output and thus act as a trigger for any other devices in the test.

To measure the voltage level of the cascade steps and the buffer output we use an oscilloscope Agilent Tech. MSOX-X 3014A with the aforementioned trigger signal that is further touched upon int able 7.1 To get all five switches, we thus did two runs of this experiment and merged the data corresponding to the trigger.

Oscilloscope	Agilent Tech. MSO-X 3014A (4-Kanal, 100MHz, 4GS/s) Impedance: 1MΩ on all measurements, if not specified otherwise
Voltage Source	Keysight N6704 (Duty Cycle 100%, Waveform DC 6.12 V, Output High Z Termination,
Current Source	Keysight N6704 (Output High Z Termination, Waveform Exponential Rise and Fall Triangle 0A to 3A to 0A,
Signal generator	Keysight N6704 (Rectangular waveform generator, 1 kHz)
PCB Probe	PCBite SP200, length: 80 cm, attenuation 10:1
Coaxial cable	RG58 with BNC connector, length: ca. 1m, attenuation 10:1
DC-Voltagesource FPGA	Output Votlage 12V, Output Current max 5A, 60W

Table 7.1.: Devices used for Measurements

7.1.1. Measurement Uncertainties

Due to the inherent inaccuracies of the sensors and components used in measurement systems, it is common to encounter various sources of error that can significantly affect the accuracy of measurements. These sources of error can arise due to a variety of factors, such as measurement noise, drift, and non-linearity, among others.

Due to these inaccuracies, we see the following sources of error in table 7.2 have an influence on measurement accuracy.

Source of Error	**Relative Value**	**Absolute Value**
Capacitive measuring cable PCB	80 cm length	18 pF
Capacitive measuring cable else	1m length, 100 pF/m	100 pF
Oscilloscope Vertical Resolution	8 Bits: Measuring range of $2^8 = 256$ possible states	$(V_{Max} - V_{Min})/256$
Oscilloscope Vertical Gain Accuracy	± 3% full scale (≥ 10 mV/div)	8 houses · V/div · 0.03
Oscilloscope DC Vertical Accuracy	25 ppm ± 5 ppm per year (ageing)	Negligible
Oscilloscope Horizontal Resolution	12 Bits with $\geq 20\mu s/dec$: Measuring range of $2^{12} = 4096$ possible states	$(t_{Max} - t_{Min})/4096$
Internal Resistance Oscilloscope	Leakage Current through Internal Resistance	Negligible

Table 7.2.: Single Measurement Errors

For the general measurement Y, one can use the gaussian law of error propagation 7.1 to calculate the error ΔY of this measurement in dependency of all uncertainties. And following this, the equations 7.2 to 7.4 summarise the measurement uncertainties used in the following experiments.

$$\Delta Y = \sum_{j=1}^{k} (\frac{\delta f}{\delta x_j} \Delta x_j) \tag{7.1}$$

$$\Delta U = \text{Vertikal Resolution} + \text{Vertikal Gain Accuracy of the oscilloscope} \tag{7.2}$$

$$\Delta I = \sqrt{(\frac{\Delta U}{R})^2 + (-\frac{U}{R^2} \Delta R)^2} \tag{7.3}$$

$$\Delta \phi = \text{Time base accuracy} \tag{7.4}$$

- The DC voltage source (GW Instek GPS-3303S) has a measurement uncertainty of less than ±0.03% (k=2). The DC voltage source may be operated with a maximum of +18 V DC for reasons of protection for the circuit. This results in an error of ±6 mV. So even if the measurement uncertainty is ±0.03%, the error would still be negligible. The DC voltage source is therefore assumed to be constant.
- The values of the components (resistors, capacitors) are only used for theoretical calculations. Therefore, the tolerances listed in chapter 4.2.4 do not play a role for the measurement uncertainty in voltage measurements.

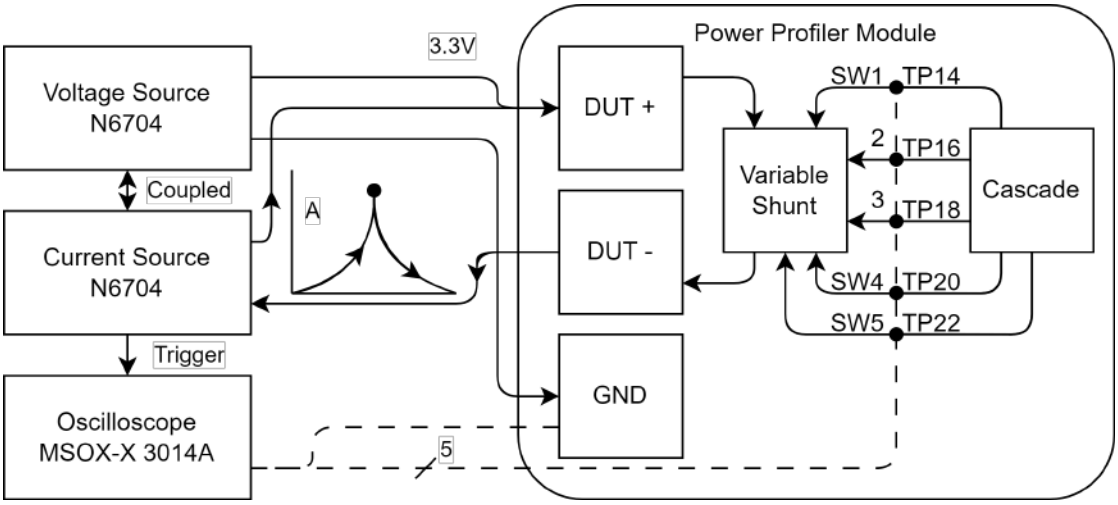


Figure 7.1.: Measurement Setup for Cascade Measurements Graphic

7.2. Measurement Setup PPM Current to Measure Switch Points

Figure 7.1 shows an illustration of the measurement setup to simulate a device under test (DUT) in the loop of the power profiler module (PPM). The voltage level between the DUT+ and ground is set to 3.3 V, and an linear increase in current is applied between the DUT positive input and the output back to the DUT via DUT-. The experiment is run for the amount of time t with a linear increase in current. Both of these points are defined in the title of the corresponding plot. The resulting voltage levels are analysed via the oscilloscope to provide insights into the behaviour of the hysteresis cascade and the resulting shunt resistance independent of the driver and ADC that follow. The simulation of this experiment can be seen in chapter 6.2.1.

Note that the oscilloscope does not have enough probes to measure all five switches. Thus two types of experiments were done one up to 7 mA and one to 1.1 A, which is sufficient to trigger the high-power mode. In table 8.1. Another experiment was done with the same setup that measures the fastest time it takes for a full cascade stepthrough from switch 1 to 5, with these results being visible in chapter 8.2.1

7.2.1. Measurement Setup PPM Current Pulse to Measure Switch Points

With the same measurement setup, another experiment calculated the time the whole cascade takes to switch into a new state. This was achieved by outputting a step-function-like current through DUT+ and DUT-. For the two experiments, a max current of 1.5

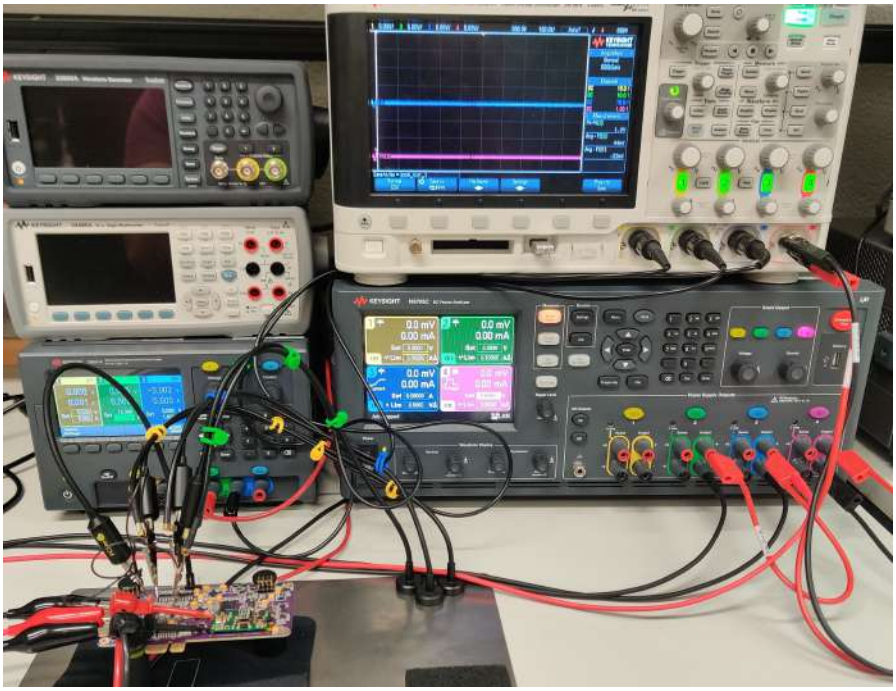


Figure 7.2.: Measurement Setup for Cascade Measurements Picture

and 0.8 was chosen to trigger the full range with high power mode and for the second one only to trigger the low power modes. The rise time of the current is described as $9.9 \cdot 10^{37} A/s$ and thus presumed instantaneous as for the timescale of this experiment. The measurements were done with 5 $\mu s/dec$ and 5 V/dec each.

7.3. Measurement Setup PPM Current ADC Output

The measurement setup for this experiment is practically the same as in chapter 7.2, but we don't need the external oscilloscope anymore, and the Current Source gets an added kelvin connection for voltage to not factor in the voltage drop over the cable into the supply calculations. Of note here was that the programmed current of the current source was mismatched with the measured current that an additional DC current probe of the N6704 measured. Thus the current probe was left in the loop, and not the programmed current was as ground truth but the displayed current of the probe.

7.4. Measurement Setup PPM Voltage Output

Figure 7.3 shows an illustration of the measurement setup to simulate a device under test (DUT) in the loop of the power profiler module (PPM). The voltage level between the DUT+ and ground is varied between the absolute maximum ratings defined for the PPM. The resulting voltage levels are read by the ADC and output to the PC where it is evaluated to provide insights into the behaviour of the two voltage measurement rails. The simulation of this experiment was not done since it is a predefined use case for the driver and ADC combination.

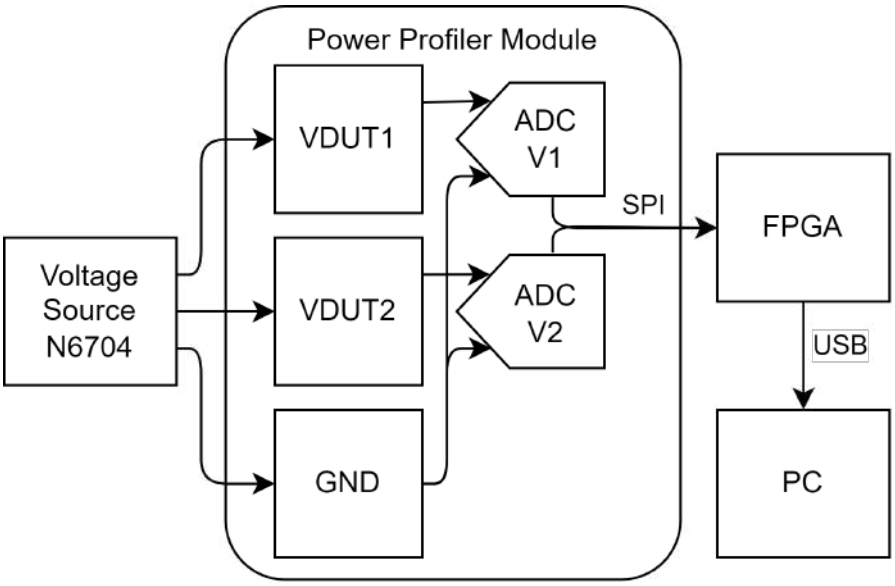


Figure 7.3.: Measurement Setup for Voltage Measurements of PPM

7.5. Measurement Setup PDM Voltage

For the power delivery module we measured the voltages selected on the basis of the most common ones used in embedded designs and compiled them in table 8.6.

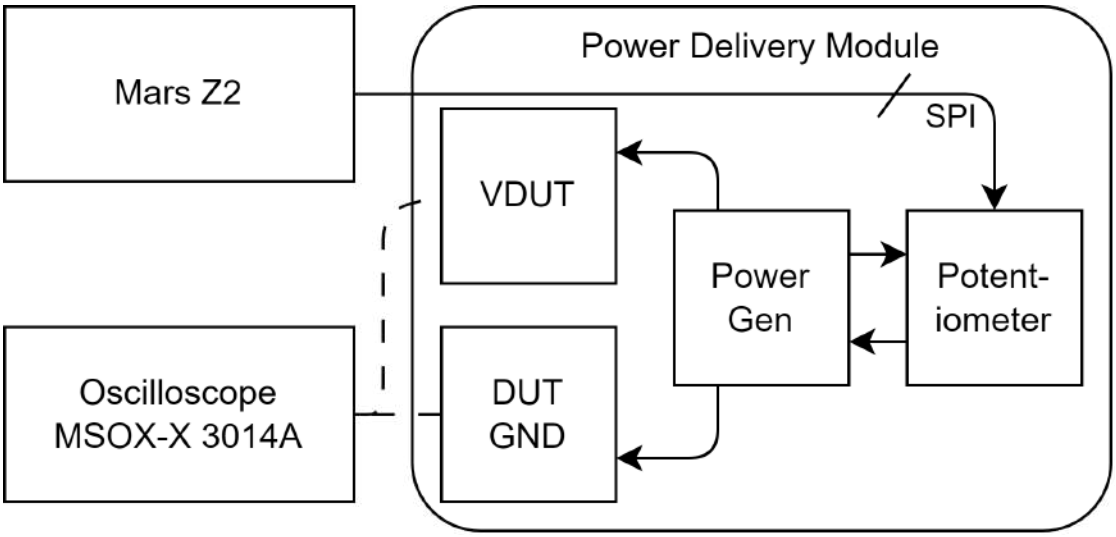


Figure 7.4.: Measurement Setup Power Generator DUT

Chapter 8

Results

In this chapter, results are displayed that will be further touched upon in the discussion in chapter 9.

8.1. Data Calibration

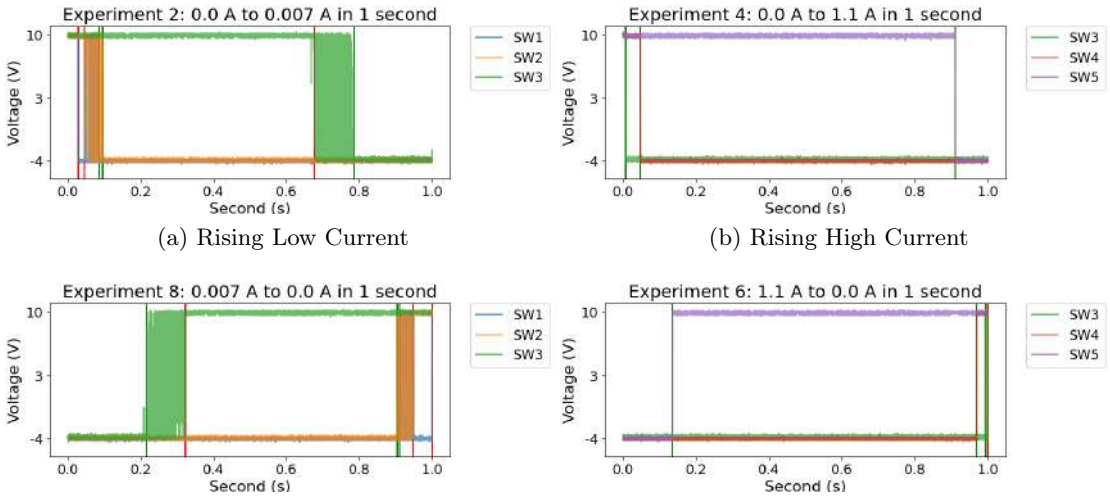
It is imperative to calibrate the measurement device since the devices can have inherent errors due to factors such as noise, drift, and non-linearity, which can result in inaccurate measurements. Calibration can help improve the accuracy and reliability of measurements by correcting these errors. However, care must be taken to not overfit the data and create a perfect-looking training set that is unusable for further measurements. One common method of calibration is to use linear regression, which is a statistical technique that finds the best-fit line that minimizes the sum of the squared errors between the predicted values and the actual values. This line can then be used to transform the measurements to the expected ground truth but one needs to avoid using data points that are outliers or have high measurement errors. Thus for all data points received, we removed every received data package where at least one of the rows deviated by three standard deviations from the mean. In a gaussian distribution, three standard deviations account for 99.7 % of data points and are known as the empirical rule in statistics and the standard in literature [17, p. 59] for such corrections.

8.2. Results PPM Current to Measure Switch Points

These are the results for the current measurement and the corresponding switching behaviour explained in chapter 7.2. Note the trend arrow in table 8.1 that indicates if the measurement was done with increasing or decreasing current. Some deltas like experiment one switch one or exp six switch three arise due to re-engagement of the cascade step when the subsequent or previous cascade step triggers, as visible in figures 8.1a / 8.1d or more noticeably in the rolling average of the same experiments in figures 8.2a / 8.2d. The biggest offender was SW3 in experiments two and eight with the low current and slow rise time. Here there appears to be quite the window for oscillation between stages two and three of the cascade. Notice the increased uncertainty for the high current measurements since it was done in the same time-space of one second.

Exp	Label	Trend	Start Current (mA)	End Current (mA)	Δ Current (mA)
1	SW1	$\nearrow$	(0.187 ± 0.002)	(0.656 ± 0.002)	(0.469 ± 0.002)
2	SW1	$\nearrow$	(0.200 ± 0.002)	(0.597 ± 0.002)	(0.397 ± 0.002)
7	SW1	$\searrow$	(0.004 ± 0.002)	(0.606 ± 0.002)	(0.601 ± 0.002)
8	SW1	$\searrow$	(0.004 ± 0.002)	(0.628 ± 0.002)	(0.624 ± 0.002)
1	SW2	$\nearrow$	(4.737 ± 0.002)	(7.000 ± 0.002)	(2.262 ± 0.002)
2	SW2	$\nearrow$	(4.744 ± 0.002)	(5.498 ± 0.002)	(0.755 ± 0.002)
7	SW2	$\searrow$	(4.734 ± 0.002)	(5.556 ± 0.002)	(0.822 ± 0.002)
8	SW2	$\searrow$	(4.743 ± 0.002)	(5.488 ± 0.002)	(0.745 ± 0.002)
1	SW3	$\nearrow$	(0.319 ± 0.002)	(0.669 ± 0.002)	(0.350 ± 0.002)
2	SW3	$\nearrow$	(0.319 ± 0.002)	(0.664 ± 0.002)	(0.345 ± 0.002)
3	SW3	$\nearrow$	(7.975 ± 0.269)	(7.920 ± 0.269)	(0.055 ± 0.269)
4	SW3	$\nearrow$	(7.975 ± 0.269)	(7.920 ± 0.269)	(0.055 ± 0.269)
5	SW3	$\searrow$	(0.550 ± 0.269)	(0.495 ± 0.269)	(0.055 ± 0.269)
6	SW3	$\searrow$	(0.605 ± 0.269)	(6.490 ± 0.269)	(5.885 ± 0.269)
7	SW3	$\searrow$	(0.358 ± 0.002)	(0.637 ± 0.002)	(0.279 ± 0.002)
8	SW3	$\searrow$	(0.356 ± 0.002)	(0.669 ± 0.002)	(0.313 ± 0.002)
3	SW4	$\nearrow$	(52.305 ± 0.269)	(52.250 ± 0.269)	(0.055 ± 0.269)
4	SW4	$\nearrow$	(52.360 ± 0.269)	(52.305 ± 0.269)	(0.055 ± 0.269)
5	SW4	$\searrow$	(32.835 ± 0.269)	(32.780 ± 0.269)	(0.055 ± 0.269)
6	SW4	$\searrow$	(32.780 ± 0.269)	(32.725 ± 0.269)	(0.055 ± 0.269)
3	SW5	$\nearrow$	(1001.935 ± 0.269)	(1001.880 ± 0.269)	(0.055 ± 0.269)
4	SW5	$\nearrow$	(1001.660 ± 0.269)	(1001.605 ± 0.269)	(0.055 ± 0.269)
5	SW5	$\searrow$	(950.400 ± 0.269)	(950.345 ± 0.269)	(0.055 ± 0.269)
6	SW5	$\searrow$	(950.345 ± 0.269)	(950.290 ± 0.269)	(0.055 ± 0.269)

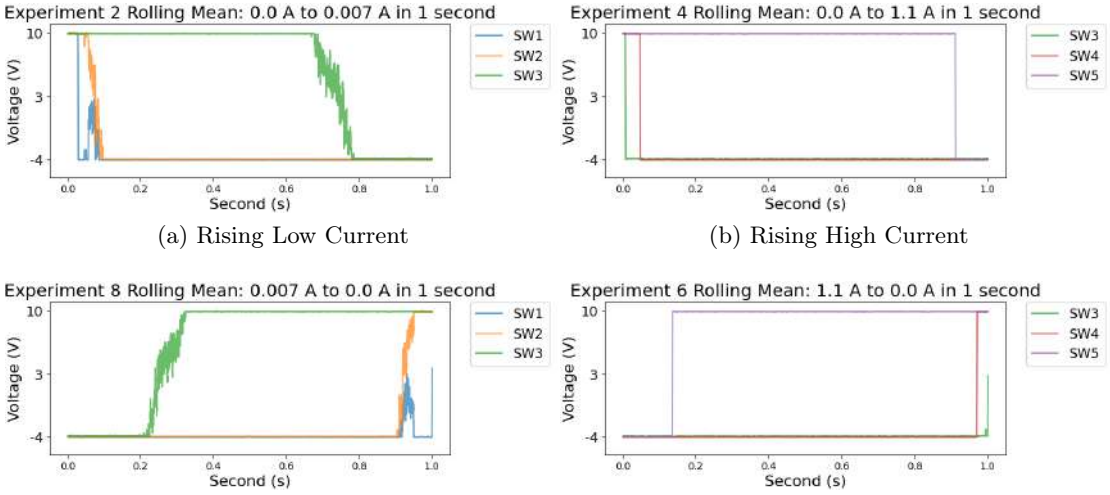
Table 8.1.: Measurements of Switching Points of Cascade



(a) Rising Low Current (b) Rising High Current

(c) Falling Low Current (d) Falling High Current

Figure 8.1.: PPM Switching Measurements



(a) Rising Low Current (b) Rising High Current

(c) Falling Low Current (d) Falling High Current

Figure 8.2.: PPM Switching Measurements Rolling Average

8.2.1. Results PPM Step Current to Measure Switch Points

In table 8.2, one can see that the high-power cascade step engages only 13.2 μs after the first cascade step engages. Interestingly one can see in figure 8.4 that SW4 never engages even though we would be in the current range for this to happen. This can only mean that the cascade pause mechanism engages faster than the cascade of the four switches takes to engage SW4. After the cascade pause engages, the input of the cascade is set to 4.1V; thus, no more state change can happen. When only the low current cascade gets agitated, the full rise time one can extract from table 8.2 is 23.5 μs which thus limits the minimum required time after a state change before any further correct measurements can be taken.

Table 8.2.: Measurements of Full Cascade Engage Times

Exp	Δ Time (us)
0	(16.4 ± 0.004)
1	(23.5 ± 0.004)

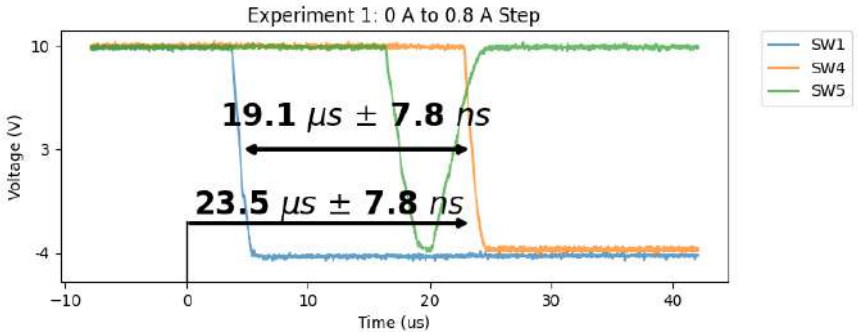


Figure 8.3.: Rising Low Current Pulse

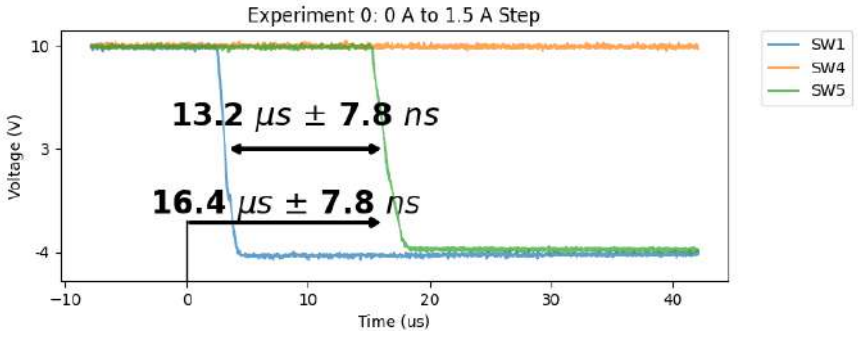


Figure 8.4.: Rising High Current Pulse

8.3. Results PPM Current Data from ADC

One can notice that all the signals are quite accurate on the average measurement but not necessarily precise. While one needs to keep in mind that to achieve the sampling rate of 100 kS/s we can still oversample the data by four, it will still only reduce the signal to noise ratio by $\sqrt{4}$. Thus a power spectral density (PSD) analysis was carried out on the smallest current signal measured for these experiments and, with that, the most noise prone. The $8\mu A$ signal showed significant frequency bumps around multiples of 11.7 kHz visible in figure 8.5. After further inspection of the prototype, it was determined that the -5 V buck converter was adding significantly more noise to the signal than anticipated. This rail is used to drive the LDOs that output the negative supply of cascade, InAmp and the driver and thus has a significant impact on the performance. For a future version, this will be necessary to rectify to increase the precision of the system and to properly utilise the performance of the ADC. Additionally the data integrity hovers around 96 % and thus for future versions cyclic redundancy check (CRC) that is a feature of the ADC, would be advisable altough the AXI stream package would need to be bigger to accommodate the eight-bit header per line or reduce the package counter.

Table 8.3.: Low Current Measurements of ADC

Current	Stage	Current Meas	σ Current Meas	Data Int (%)	Acc (%)	Prec (%)
8.000 μA	0	8.053 μA	3917.30 nA	95.14	0.66	48.64
15.000 μA	0	14.948 μA	3578.45 nA	96.94	0.35	23.94
25.000 μA	0	24.972 μA	3558.18 nA	97.23	0.11	14.25
35.000 μA	0	35.016 μA	3566.42 nA	97.23	0.05	10.18
45.000 μA	0	45.010 μA	3575.37 nA	97.15	0.02	7.94
150.000 μA	1	149.865 μA	27957.52 nA	96.53	0.09	18.66
250.000 μA	1	250.109 μA	27967.70 nA	97.51	0.04	11.18
350.000 μA	1	350.242 μA	27757.89 nA	97.96	0.07	7.93
425.000 μA	1	424.784 μA	28197.03 nA	96.34	0.05	6.64
757.000 μA	2	757.535 μA	165152.50 nA	97.76	0.07	21.80
1.514 mA	2	1.513 mA	178.16 μA	96.39	0.07	11.78
2.523 mA	2	2.524 mA	178.89 μA	96.66	0.06	7.09
3.532 mA	2	3.533 mA	177.98 μA	96.19	0.02	5.04
4.289 mA	2	4.288 mA	181.18 μA	97.06	0.02	4.23
8.257 mA	3	8.255 mA	326.44 μA	95.18	0.03	3.95
16.514 mA	3	16.525 mA	328.22 μA	97.27	0.07	1.99
27.523 mA	3	27.511 mA	331.74 μA	96.06	0.04	1.21
38.532 mA	3	38.528 mA	331.88 μA	96.88	0.01	0.86
46.789 mA	3	46.796 mA	332.57 μA	96.72	0.01	0.71
155.316 mA	4	155.497 mA	362.40 μA	97.00	0.12	0.23
310.631 mA	4	310.700 mA	357.24 μA	96.54	0.02	0.11
517.719 mA	4	517.344 mA	381.98 μA	97.50	0.07	0.07
724.807 mA	4	724.583 mA	397.83 μA	96.61	0.03	0.05
880.122 mA	4	880.470 mA	409.14 μA	97.08	0.04	0.05
1.000 A	5	1.002 A	0.51 mA	97.12	0.21	0.05
1.500 A	5	1.502 A	0.52 mA	96.88	0.13	0.03
2.000 A	5	2.002 A	0.52 mA	96.88	0.10	0.03
2.500 A	5	2.502 A	0.53 mA	96.26	0.08	0.02
3.000 A	5	3.002 A	0.55 mA	97.19	0.07	0.02

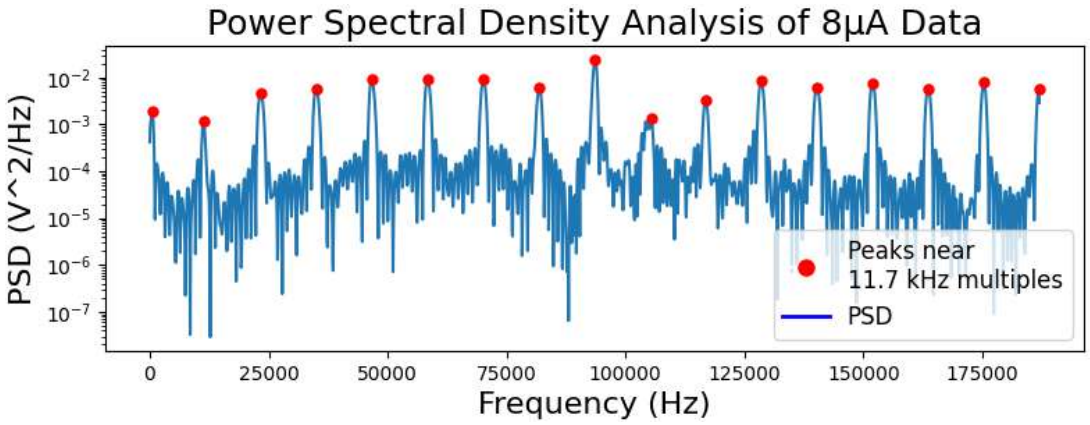


Figure 8.5.: Caption

8.4. Results PPM Voltage Data from ADC

Two of the four ADC are designated for voltage measurements, V1 being the voltage on the same connection to which the current probe VDUT+ is connected. The ADC was calibrated with linear regression of the measurement points versus the ideal values to get the intercept and slope values (linear and multiplicative) to fit the data.

Table 8.4.: Voltage Measurements One of ADC

Voltage	V1 (V)	σ V1 (mV)	Data Int (%)	Accuracy (%)	Precision (%)
0.8V	0.79683	0.14	97.01	0.398	0.018
1.2V	1.19807	0.13	97.14	0.161	0.011
1.8V	1.79989	0.14	96.70	0.006	0.008
2.8V	2.80296	0.14	98.07	0.106	0.005
3.3V	3.30615	0.12	97.11	0.186	0.004
4.5V	4.50358	0.12	97.23	0.079	0.003
5.0V	4.99846	0.13	96.12	0.031	0.003
5.4V	5.39407	0.13	97.74	0.110	0.002
5.5V	5.40700	0.00	93.59	1.720	0.000

Table 8.5.: Voltage Measurements Two of ADC

Voltage	V2 (V)	σ V2(mV)	Data Int (%)	Accuracy (%)	Precision (%)
0.8V	0.79683	0.14	97.01	0.398	0.018
1.2V	1.19807	0.14	97.14	0.161	0.011
1.8V	1.79989	0.14	96.70	0.006	0.008
2.8V	2.80296	0.14	98.07	0.106	0.005
3.3V	3.30615	0.12	97.11	0.186	0.004
4.5V	4.50357	0.12	97.23	0.079	0.003
5.0V	4.99846	0.13	96.12	0.031	0.003
5.4V	5.39407	0.13	97.74	0.110	0.002
5.5V	5.40662	0.00	93.59	1.727	0.000

8.5. Results PDM VDUT Output

In most cases, the dispersion of the power delivery module (PDM) results is around 1%, and only the rough steps around the highest voltages indicate an opportunity for improvement in version two. The lowest possible voltage is by design at 0.86 V instead of 0.8 V since we didn't include two more potentiometers to achieve the needed resistances for the last 0.06 V of the range. Lastly, these values were only inferred from the ideal calculation. The potentiometer has a fixed uncertainty that could be factored out with the calculation and application of a calibration table.

Table 8.6.: Power Delivery Voltage Output Versus Expected

VDUT	Bit	Exp	Average (V)	σ (mV)	V/dec	ms/dec	Acc (%)	Prec (%)
0.86	1023	7	(0.857 ± 0.004)	21.8	1	100	0.385	2.547
1.20	230	9	(1.198 ± 0.004)	22.5	1	100	0.172	1.880
1.30	186	10	(1.301 ± 0.004)	22.2	1	100	0.079	1.706
1.80	92	2	(1.807 ± 0.004)	21.9	1	100	0.360	1.213
2.30	59	3	(2.312 ± 0.004)	23.5	1	100	0.536	1.015
2.70	45	8	(2.712 ± 0.004)	25.8	1	100	0.460	0.950
3.30	32	1	(3.316 ± 0.004)	24.4	1	100	0.495	0.736
3.50	29	4	(3.517 ± 0.004)	26.9	1	100	0.495	0.764
5.00	15	5	(5.009 ± 0.004)	30.7	1	100	0.187	0.612
5.50	12	6	(5.585 ± 0.004)	31.3	1	100	1.524	0.560

Chapter 9

Discussion

With these results, it is apparent that the power profiler module, power delivery module (PDM), and by extension, the device under test setup performs its functionality that we will discuss more precisely in the following sections.

9.1. Power Profiler Module

The PPM employs a novel way of measuring in different current bands from a maximum of 10 A to a calculated practical minimum of 310 pA representing a current measurement range of 210 dB, outperforming related work like Sigrist et al. [3] with 165 dB or industrial devices containing similar switching circuits like the Nordic Power Profiler with 160 DB with more comparisons in figure 9.1. This prototype could not wholly realise this range since power spectral density (PSD) shown in figure 8.5 revealed noise pollution on the -5 V supply, inhibiting this range on the lower end. This induces a precision of 50% on the lowest measurement of 8 μA while maintaining an accuracy of 0.66%. This error can be fixed in future versions without redesigning any novel analogue circuits in this prototype. Additionally, as seen in the results and, more specifically, figure 8.1a and 8.1c, the auto-ranging does not yet behave in a bistable way without oscillation for every single current. However, it only represents about two mA over the entire 10 A range or 0.02% of the full range.

One could quickly surmise that the fault for these oscillations is that the hysteresis rise and fall voltages are wrongly dimensioned as we did initially. After further study and simulation, we theories that the culprit lies in the used MOSFETs for the variable shunt resistance. For ease of development, we installed the same MOSFET type for each of the five stages designed for a continuous drain current of 20 A. With this characteristic to sustain our maximum rated current comes the tradeoff of a more prominent channel

width and a significantly higher input capacitance which changes the RC time constant. Another factor for this is the current limiting resistor that connects to the gate of these MOSFETs. We saw in the simulation chapter 6.2.2 that fewer oscillations can be measured with the increase of these limiting resistors, though with the tradeoff of a slower switching time and resulting slower feedback. With this knowledge, future work must include distinct MOSFETs designed for the maximum expected current drain at that stage.

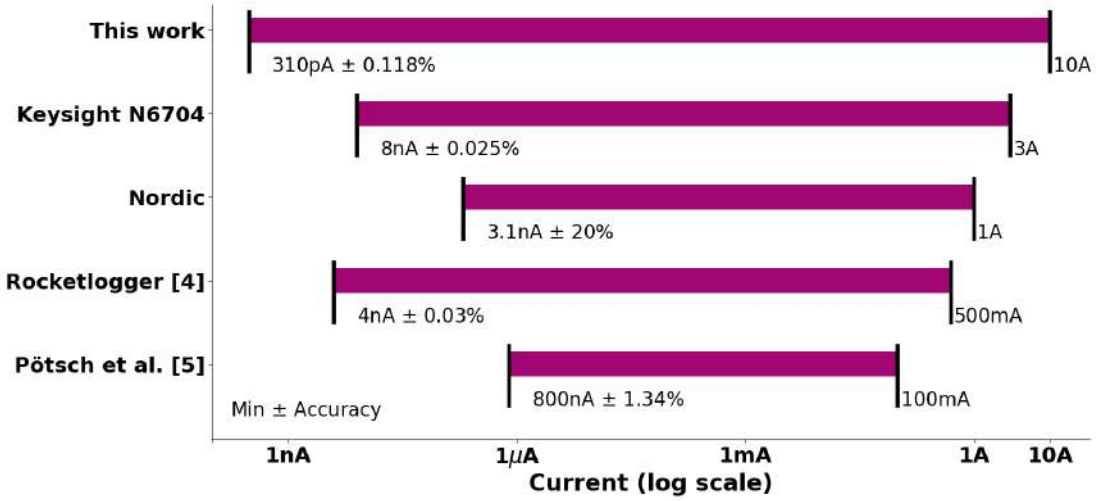


Figure 9.1.: Current Ranges State of the Art

Switching Times

This measuring circuit automatically switches between five stages with a maximum switching time of 23.5 μs for complete stability over all five stages, meaning 90% on the last stage. For every single stage, that gives us a switching time of 5.88 μs that is on the same timescale as 1.5 μs from Sigrist et al. [3]. Measuring at full speed in high precision mode at 187 kS/s allows us not to invalidate any measurements when switching only over one stage. Still, any additional switches must be handled in software by invalidating up to three measurements after the switch takes place, depending on the number of stages triggered. With the proposed solution of using different MOSFETs per stage and thus limiting the channel width and its corresponding RC time constant, one could also decrease the switching time of the lower cascades in future work.

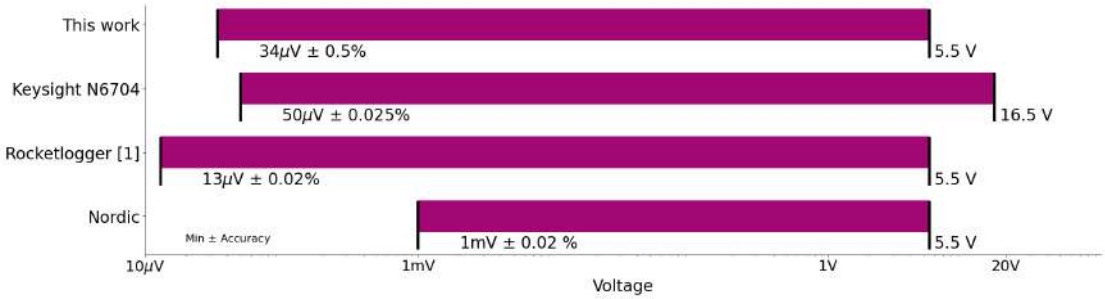


Figure 9.2.: Voltage Ranges State of the Art

Voltage Measurement

The voltage measurements over the PPM as seen in chapter 8.4 show a high accuracy of less than half a per cent for all measurements and an even greater precision below 2‰for both voltage measurement nodes. In figure 9.2 one can see a graphical comparison for these ranges with realted work. Sigrist et al. [3] was able to measure voltage with noise of 8 μV RMS which equates to a precision of 0.05‰outperforming the PPM since it is equiped with coaxial measurement connectors. A device that also uses 2.54 mm jumper connectors, the Analog Discovery 2 has a best-case accuracy of 10 mV ± 0.5% corresponding to an accuracy of 1 to 4 %, and the Nordic Power Profiler Kit 2 can even have an accuracy of 10%. Both channels appear to be saturating at just above 5.4 V, indicating a misalignment of the measurement ranges. This was fixed with linear scaling of the data but failed in the saturated regions. Thus this module can thus reliably supply up to 5.4 V measurements in its current configuration.

9.2. Power Delivery Module

The PDM power delivery can supply a total of 20 watts with a voltage accuracy of 5‰as recorded in table 8.6. The standard deviation of the measurements increased only marginally over the entire range, indicating a generally fixed uncertainty of 20 mV with smaller voltage-dependent factors that shows itself in a 2.5% precision at the lower voltage level that only decreases to 6‰over the entire range. With these 20 W, we outperform the 2.1 W and 700 mA from the Analog Discovery 2 and the 5 W and 1 A from the Nordic Power Profiler over a similar full range. The Analog Disc has a better accuracy at about 10 mV, with the Nordic not mentioning its accuracy. One shortcoming of this design is the lower input impedance that pulls current from the DUT. The voltage divider should be preceded by a follower operational amplifier (OpAmp) before the input voltage for a future version.

9.3. Data Interjection

The device can currently interact with four SPI second devices with a maximum of 15.6 MHz transfer speed. The feature is currently implemented based on the RTOS timers that limit the frequency of instructions to 1 ms or 1 kHz with no limit on the instruction size. This enables the prototype to reliably interact with any second devices while keeping the whole system galvanically isolated. Since no dedicated module was built for this feature, there is currently no support for other protocols, but this would present itself for future work to increase the feature set of the whole DUT setup.

9.4. Summary Table

Work	Current Max (Meas)	Current Min (Meas)	Sample Rate (S/s)	Current Max (Delivery)	Switch Speed (1 Stage)	Switch Speed (All)	Number of Switches	Voltage Max (Meas)	Voltage Min (Meas)	Can Log Data	Can Inject & Receive Data
This Work	**10A**	**310pA**	**187k**	**10A**	**5.88μs**	**23.5μs**	**5**	**5.5V**	**23μV**	✓	✓
RocketLogger [3]	500mA	4nA	64k	×	1.5μs	×	1	5.5V	13μV	✓	✓
Pötsch et al. [5]	100mA	800nA	125k	×	?	×	1	×	×	✓	×
Nordic [2]	1A	3.1nA	100k	1A	?	?	4	5.5V	1mV	✓	×
Keysight [18]	3A	8nA	200k	3A	?	?	?	16.5V	50μV	✓	×

Table 9.1.: Summary of Keypoints of this Work versus Related Work.

Chapter 10

Conclusion

Prior Research has documented a multitude of options to measure a high range of current and to implement these techniques into a complete package to execute a proper hardware in the loop (HIL) testing. This thesis extended previous techniques by introducing a novel approach for adding a high-power mode that can halt the already long cascade, unlike previous research that generally focused on only one stage transition [4, 5, 3]. In contrast, this approach allowed for improved functionality by extending the current measurement ranges from 165 dB as shown in Sigrist et al. [3] to a range of 210 dB. In addition, this work is able to independently supply a device under test (DUT) with power up to 20 W and additional stimulus data over SPI and its recorded answers. With this combination of measurement devices and power delivery possibilities, this work shows a complete HIL package that can be extended by stacking more modules of the desired type. This enables the testing of low-power embedded devices while simultaneously providing and measuring the high inrush current drawn by FPGAs, all within a modular framework designed for workstation compatibility.

In the future, the developed prototype is expected to serve as a foundation for incorporating additional features, thanks to its modular design, while already functioning as a hardware in the loop (HIL) testbed.

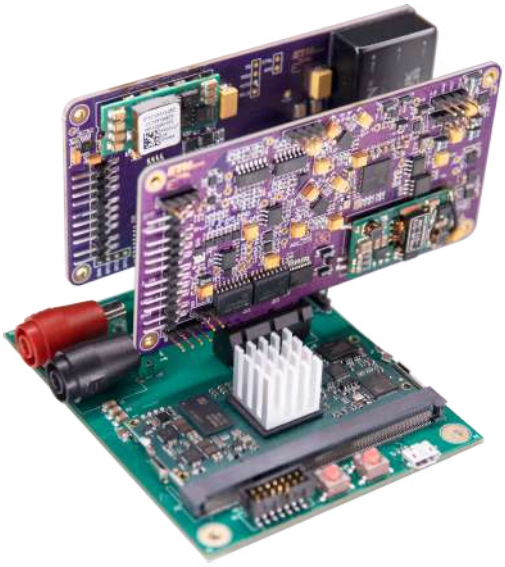


Figure 10.1.: Full Prototype with PPM, PDM and Interposer

10.1. Future Work

- **Noise on -5 V rail:** Although low current measurements demonstrated 0.66% accuracy, the noise-laden power rail significantly impacted the precision of individual low-power measurements. To address this, further noise-cleaning should be implemented for power rails supplying measurement devices, starting with the most significant offender, the -5 V buck converter.
- **Oscillation of small current ranges:** As discussed in Chapter 9.1, employing universal MOSFETs adversely affects lower current bands, causing oscillation during switching. This is due to the larger-than-necessary width of the MOSFET, which negatively impacts the RC time constant governing switching behaviour.
- **Voltage Measurement Impedance:** The voltage divider employed for scaling input voltage to ADC saturation levels exhibits low impedance, resulting in power drain from the DUT. A high-impedance solution, such as a follower op-amp, would be more suitable.
- **Data Interposer Extensions:** The Interposer currently can only stimulate the SPI dataprotocol. Developing a dedicated module to stimulate additional protocols would be beneficial for creating a comprehensive hardware in the loop testbed.

Appendix A

System Setup Appendix

A.1. Python GUI and Driver

To operate the FPGA and modules without reflashing the whole setup, the interposer is fitted with a micro USB port for connection to a PC. On the PC a tkinter based python GUI can be used to interact with the task_spawner embedded into FreeRTOS, set the VDUT output voltage, start the ADC data stream and a small text editor to change the commands and their timings that one wants to send to the device under test from the testbench for an entire test run. To use this GUI as visible in figure A.1, have the USB connection flashed with the libusb driver, which can be achieved with the Zadig tool. Note that the graphed data is not correctly scaled. The correct scaling was only applied during data evaluation but never reimplemented into the guy. Most importantly, because of this, the correct stage does not get taken into account on the low current graph.

A.2. Programming of AD7134

The registers 0x16 to 0x1C notably store the ODR integer and fractional portion of the decimation rate used to set the ODR output frequency based on the master clock frequency. We employ an MCLK of 48 MHz and would like a sample rate of 374 kSps. This creates the decimation rate in equation A.1. All other changes to the register are in table A.1.

$$Decimationrate = \frac{MCLK}{ODR} = \frac{48MHz}{374kSps} = 128.36... = 80.579D6EE1_{16} \tag{A.1}$$

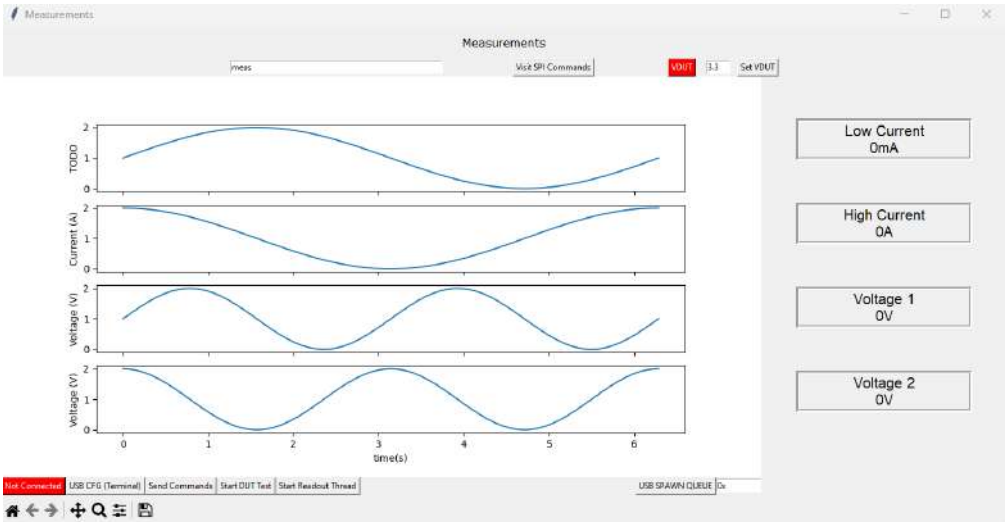


Figure A.1.: Python GUI to interact with the testbench

- **Text Field (meas):** Name of files that will be saved.
- **Visit SPI Commands:** Opens text editor for DUT commands.
- **VDUT:** Enables or disables power output of PDM that is set to voltage in the following text field.
- **Set VDUT:** Programmes potentiometer so that PDM outputs correct voltage. Can be done while VDUT is outputting.
- **(Not) Connected:** Connect to board. Automatically detects working board with USB Vendor 0x03FD (Xilinx, Inc) and product id 0x0404.
- **USB CFG (Terminal):** Outputs USB configuration of connected board to terminal.
- **Send Commands:** Sends commands in the document visible via the "Visit SPI Commands" button. These commands get saved on the device for later use.
- **Start DUT Test:** Starts readout and uses commands previously sent.
- **Start Readout Thread:** Starts measurements but no commands are sent to DUT.
- **USB Spawn Queue:** Ability to start any task in the FreeRTOS task manager via a HEX code in the text field on the right. Mostly for debugging.

Adr	Ofst	Name	Val	Comment
0x00	0b6	ADDRESS ASCENSION BIT	0b1	Used in conjunction with streaming mode, address ascension causes sequential register addresses to ascend in order.
0x01	0b7	SINGLE INSTR	0b0	Only used in streaming mode. Turns on streaming.
0x0E	0b0	STREAM MODE	0x48	Only used in streaming mode. Depth of loop set to full register size.
0x10	0b0	XCLKOUT EN	0b1	XCLKOUT enabled.
0x11	0b4	Data Packet Frame	0b10	24-bit ADC data only, no CRC.
0x12	0b0	Digital Interface Format	0b10	Quad channel parallel output mode. Each ADC channel has a dedicated data output pin.
0x15	0b3	Device Status	0x07	DCLK is in free running mode. / DCLK is output. / Master mode: ODR is output.
0x16	0b0	Decimation Rate INT	0x80	See equation A.1.
0x19	0b0	Decimation Rate FRAC	0xE1	See equation A.1.
0x1A	0b0	Decimation Rate FRAC	0x6E	See equation A.1.
0x1B	0b0	Decimation Rate FRAC	0x9D	See equation A.1.
0x1C	0b0	Decimation Rate FRAC	0x57	See equation A.1.
0x20	0b0	GPIO DIR Ctrl	0x0F	Configures GPIO 0 to 3 to be outputs.
0x25	0b3	Diagnostic Ctrl	0b1	Creates MCLK redout register on address 0x3F.

Table A.1.: Programming of the Register Bank

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

CENTER FOR PROJECT-BASED LEARNING

Task Description for a Master Thesis on

Design and Validation of a Combined Power Tracer and Sensor Emulator for the Evaluation of Embedded Hardware/Software System Designs

at the Departement of Information Technology and Electrical Engineering

for

Nando Galliard
gnando@student.ethz.ch

Advisors:	Christian Vogt, christian.vogt@pbl.ee.ethz.ch Federico Villani, federico.villani@pbl.ee.ethz.ch
Professor:	Prof. Dr. Florian Dörfler, doerfler@control.ee.ethz.ch
Handout Date:	20.09.2022
Due Date:	20.03.2023

Project Goals

Power profiling is an important measurement to optimize both software and hardware of devices during development. Especially for hardware/software co-design, where tasks can either be implemented in software on processor cores or in hardware logic (programmable or static) good knowledge of power consumption and latency/memory trade-offs between the implementations is needed.

Power profiling is widely available commercially, for example by Keysight, National Instruments and also as open source demonstrators, for example by Nordic Semiconductor[1] or EEV[2]. However, all of these devices are optimized for single channels.

In order to properly evaluate different hardware software trade-offs in microcontroller/FPGA combinations, at least 3 channels would be needed to measure the power draw (microcontroller power supply, FPGA general power and FGPA core supply). In addition, the design trade-offs can only be measured reliable with known input signals to the system as well as known signal timing.

Therefore, the goal of this thesis is the design and validation of a system capable of recording up to 6 power supply channels (current and voltage) concurrently as well as the capability to emulate standard sensor interfaces (e.g. SPI) with pre-defined virtual sensor signals and interpret results of the device under test. Furthermore, as scientific outlook, the thesis will show the viability of this developed device by measuring the power trade-offs in power consumption and latency in a simple hardware software co-design consisting of a low power microcontroller and FPGA.

Tasks

The project will be split into multiple phases, as described below:

Phase 1 (Month 1)

Focus on the introduction to the topic, top level design and component selection.

1. Investigate the state-of-the-art of the single blocks (power supply, high dynamic range current measurement, sensor emulation) and define the basic hardware requirements with your supervisors
2. Design a top level schematic and hardware/firmware design concept
3. Identify and simulate state of the art power measurements and power supply circuits with spice
4. Document the chosen top level design in terms of analog and digital hardware, firmware as well as computer software to store and view the measurements

[1] https://www.nordicsemi.com/Products/Development-hardware/power-profiler-kit
[2] https://www.eevblog.com/product/ucurrentgold/

Phase 2 (Month 2-3)

Focus on the hardware design and evaluation, including necessary firmware.

1. Design the hardware and firmware for the power supply, power measurement and sensor emulation
2. Build and validate the design with respect to accuracy, repeatability, data throughput and power consumption

Phase 3 (Month 4-5)

Focus on computer software side as well as a demo application

1. Implement the computer software to record and visualize the measured data
2. Setup a demo application on a microcontroller/FPGA device to showcase the use of your developed device

Phase 4 (Month 6)

Focus on finish thesis

1. Clean up documentation, hardware schematics, firmware, software and write report
2. Prepare final presentation

Milestones

By the end of the thesis the following Milestones should be completed:

- State of the art summarized for: variable power supply, power measurement and sensor emulation
- Top level block diagram of the device and main components for computer software
- All interfaces and data rates defined
- Simulation results of analog circuit parts
- Hardware prototype of the device
- Measurement report and validation of accuracy and function
- Working computer software to record power measurements and set configurations (such as power supply voltage, sampling rate, sensor emulation type).
- A simple algorithm on a micro controller and on an FPGA, to compare power requirement of both.

- Fully working device and software
- Cleaned final design and documentation
- Final report and presentation.

Project Organization

During the thesis, students will gain experience in the independent solution of a technical-scientific problem by applying the acquired specialist and social skills. The grade is based on the following: Student effort, thoroughness and learning curve; Results in terms of quality and quantity; final presentation and report; documentation and reproducibility. All theses include an oral presentation, a written report and are graded. Before starting, the project must be registered in myStudies and all required documents need to be handed in for archiving by PBL.

Weekly Report

There will be a weekly report/meeting held between the student and the assistants. The exact time and location of these meetings will be determined within the first week of the project in order to fit the students and the assistants schedule. These meetings will be used to evaluate the status and document the progress of the project (required to be done by the student). Beside these regular meetings, additional meetings can be organized to address urgent issues as well. The weekly report, along with all other relevant documents (source code, datasheets, papers, etc), should be uploaded to a clouding service, such as Polybox and shared with the assistants.

Project Plan

Within the first month of the project, you will be asked to prepare a project plan. This plan should identify the tasks to be performed during the project and sets deadlines for those tasks. The prepared plan will be a topic of discussion of the first week's meeting between you and your assistants. Note that the project plan should be updated constantly depending on the project's status.

Final Report and Paper

PDF copies of the final report written in English are to be turned in. Basic references will be provided by the supervisors by mail and at the meetings during the whole project, but the students are expected to add a considerable amount of their own literature research to the project ("state of the art").

Final Presentation

There will be a presentation (15 min presentation and 5 min Q&A for BT/ST and 20 min presentation and 10 min Q&A for MT) at the end of this project in order to present your results to a wider audience. The exact date will be determined towards the end of the work.

References

Will be provided by the supervisors by mail and at the meetings during the whole project.

Place and Date _____ Signature Student _____

Bibliography

[1] N. Brayanov and A. Stoynova, "Multi-microcontroller emulation of sensors, actuators and systems for flexible integration of complex devices," in *2018 41st International Spring Seminar on Electronics Technology (ISSE)*. IEEE, pp. 1–6.

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Declaration of originality

The signed declaration of originality is a component of every semester paper, Bachelor's thesis, Master's thesis and any other degree paper undertaken during the course of studies, including the respective electronic versions.

Lecturers may also require a declaration of originality for other written papers compiled for their courses.

I hereby confirm that I am the sole author of the written work here enclosed and that I have compiled it in my own words. Parts excepted are corrections of form and content by the supervisor.

Title of work (in block letters):

Design and Validation of a Combined Power Tracer and Sensor Emulator for the Evaluation of Embedded Hardware/Software System Designs

Authored by (in block letters):

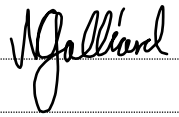
For papers written by groups the names of all authors are required.

Name(s):	**First name(s):**
Galliard	Nando

With my signature I confirm that

- I have committed none of the forms of plagiarism described in the 'Citation etiquette' information sheet.
- I have documented all methods, data and processes truthfully.
- I have not manipulated any data.
- I have mentioned all persons who were significant facilitators of the work.

I am aware that the work may be screened electronically for plagiarism.

Place, date	**Signature(s)**
02.03.2023	

For papers written by groups the names of all authors are required. Their signatures collectively guarantee the entire content of the written paper.

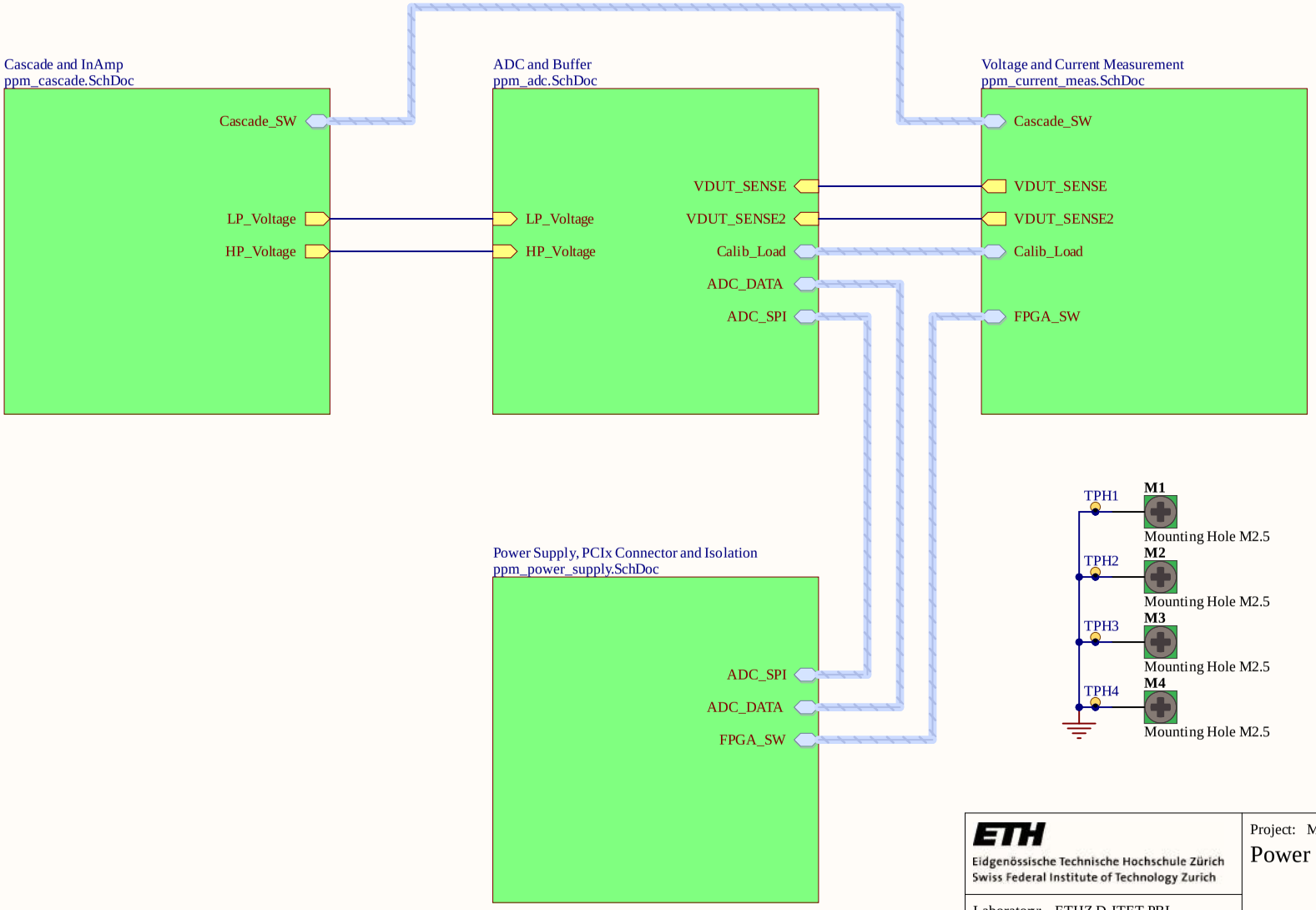
Appendix D

File Structure

The thesis files are divided up into four different repositories. The most critical file locations are marked in this chapter.

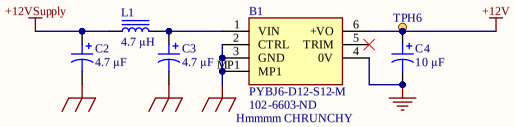
- `Boardfiles` ..... Containing all board documents for the three developed boards
  - `Power Profiler Module` ..... Files for creation of PPM
  - `Power Delivery Module` ..... Files for creation of PDM
  - `Interposer` ..... Files for creation of DIM
- `Documentation` ..... Containing measurement data and everything meetings
  - `Measurements` ..... Folder that contains all measurements and simulations
    - `Data` ..... Untouched and graphed measurement data
    - `Python` ..... Project Folder
    - `Simulations` ..... Untouched and graphed simulated data
  - `Report` ..... Folder that contains Report files and figures
- `MT_Firmware` ..... Contains the Vitis and Vivado projects
  - `Python` ..... Python Code Folder
    - `guy.py` ..... User Interface to interact with the board, see chapter A.1
  - `VitisWorkspace` ..... Workspace for firmware
    - `MA-ZX2-10-2I-D9` ..... Project Folder
      - `Mars_ZX2_ST3.xpr` ..... Vivado project file
  - `Vivado` ..... Workspace for bitstream
    - `Hello_world` ..... Application folder
    - `Hello_world_system` ..... System folder
    - `Mars_ZX2_Interposer` ..... Board folder
- `Spice of life` ..... Contains the ADS simulation workspace
  - `Nordic_Current_Sense_wrk` ..... Contains Simulation Workspace
    - `Automatic_Switching_v5.dds` ..... Final simulation file
  - `Python` ..... Contains cascade calculation helper functions
    - `cascade_helper.ipynb` ..... Notebook to calculate everything cascade

Power Profiler Module

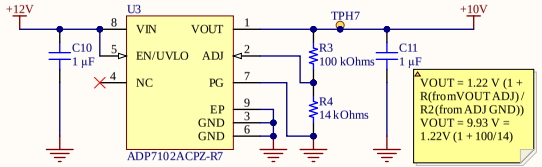


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: Master Thesis Power Profiler Module
Laboratory: ETHZ D-ITET PBL Date: 04/03/2023 16:16:36 Rev: 1 Variation: [No Variations]	Drawn By: Nando Galliard Checked By: Federico Villani
File: pmm_top.SchDoc	Sheet: 1 / 5

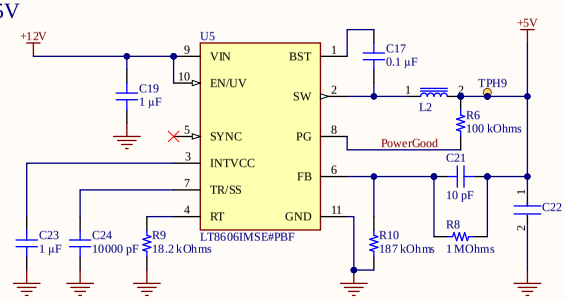
12V DCDC Isolation



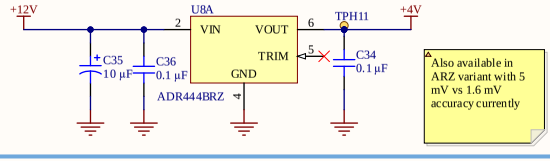
10V



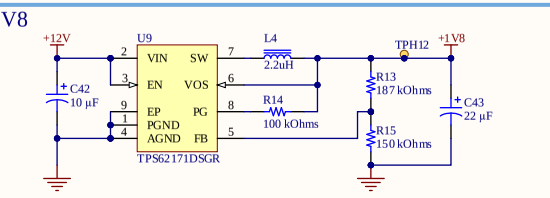
5V



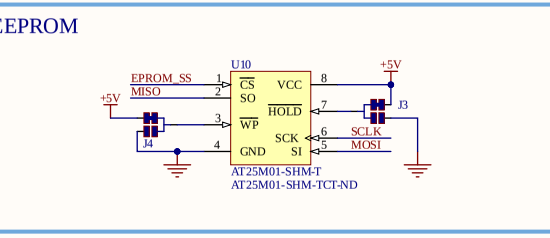
4.096V ADC_In



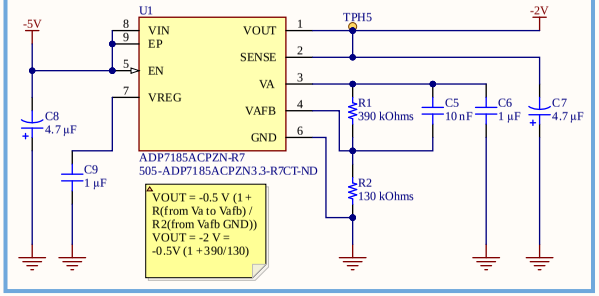
1V8



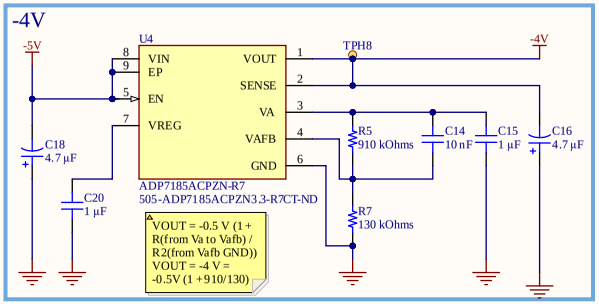
EEPROM



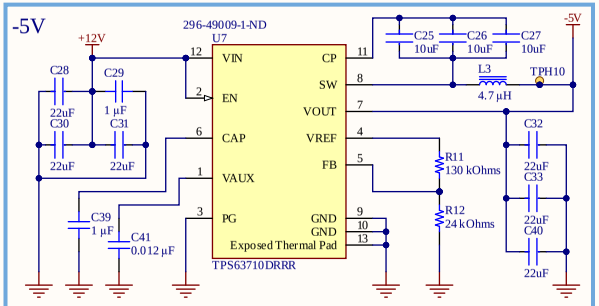
-2V



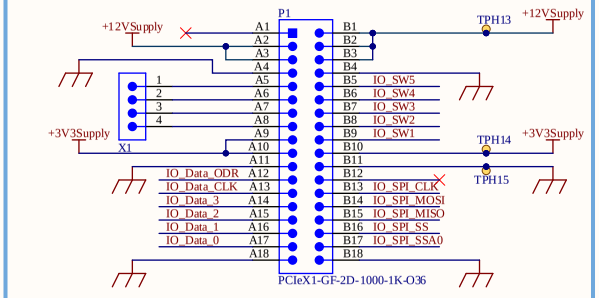
-4V



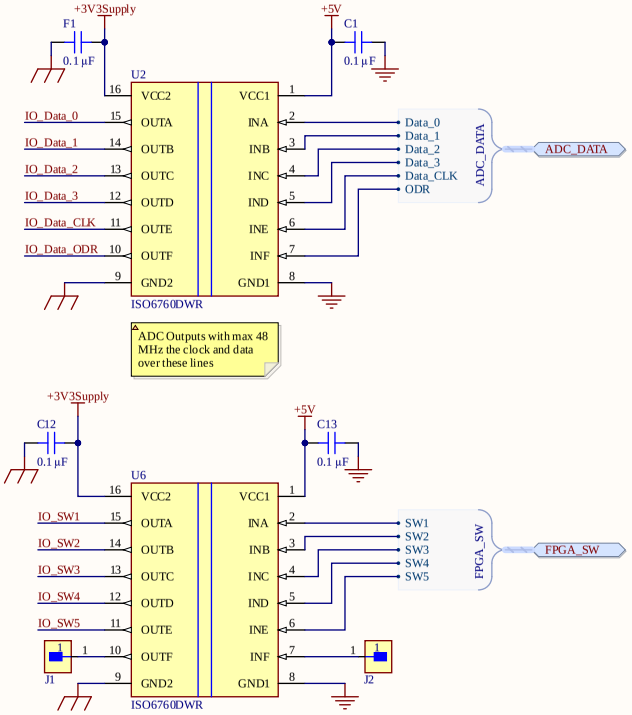
-5V



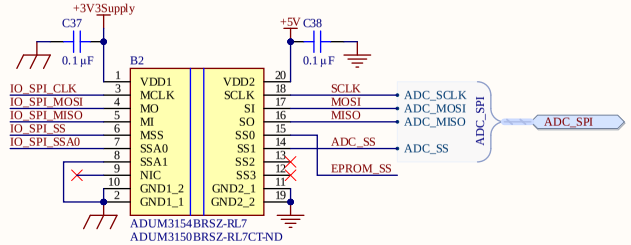
PCI X1 Connector



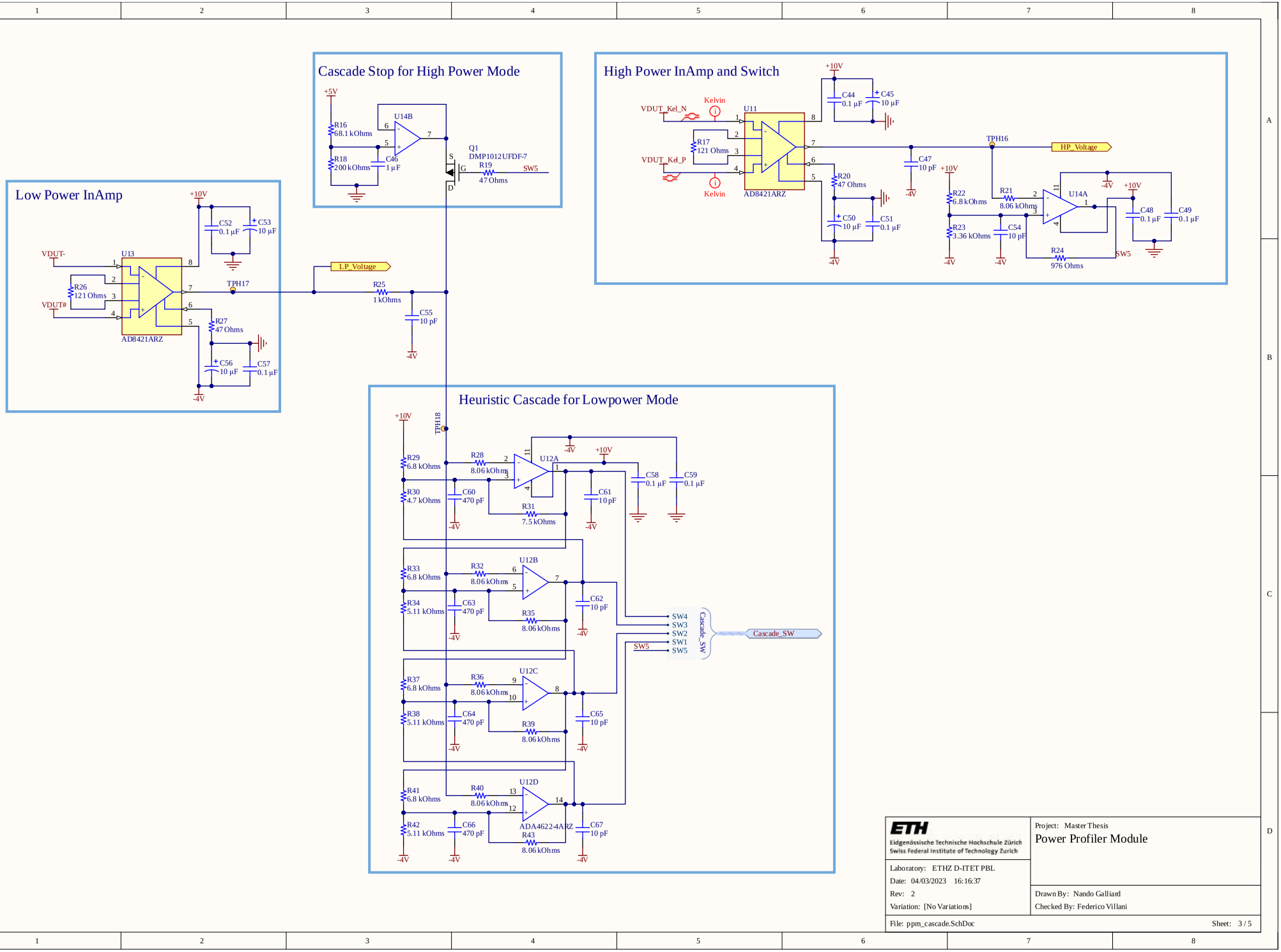
Data OUT from ADC to FPGA



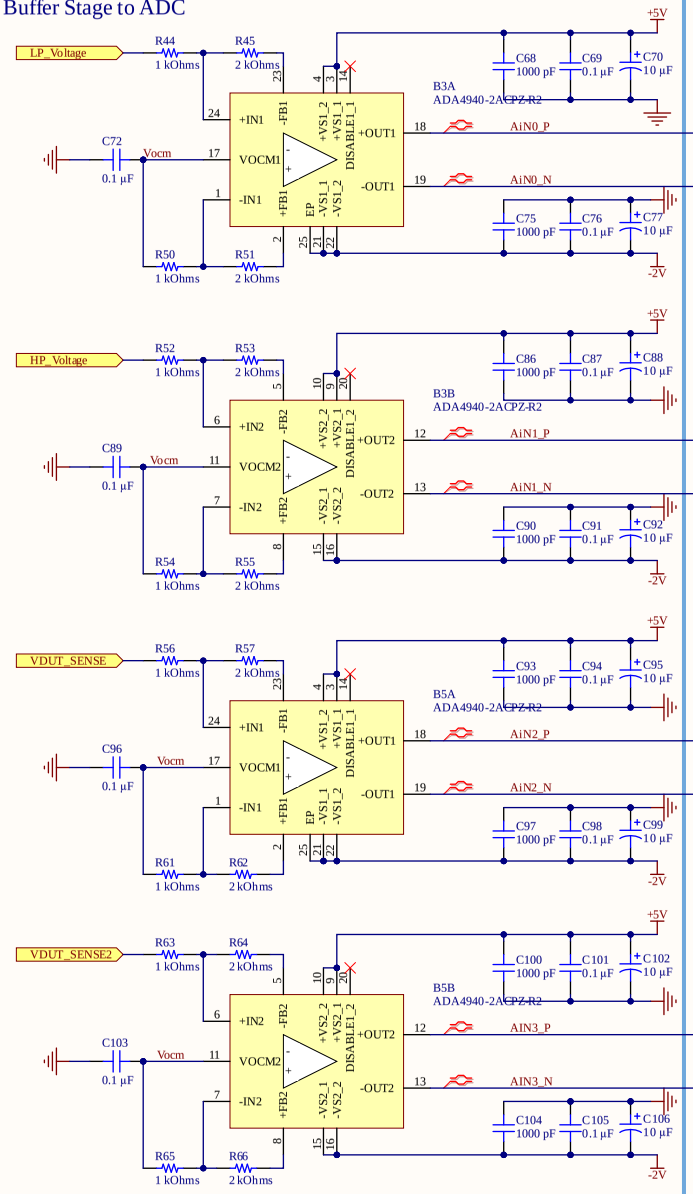
SPI I/O ADC to FPGA



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: Master Thesis **Power Profiler Module**
Laboratory: ETHZ D-ITET PBL Date: 04/03/2023 16:16:37 Rev: 2 Variation: [No Variations]	Drawn By: Nando Galliard Checked By: Federico Villani
File: ppm_power_supply.SchDoc	Sheet: 2 / 5


Cascade Stop for High Power Mode
+5V
R16
68.1 kOhms
U14B
R18
200 kOhms
C46
1 µF
Q1
DMP1012UFDF-7
R19
47 Ohms
SW5
High Power InAmp and Switch
+10V
C44
0.1 µF
C45
10 µF
VDUT_Kel_N
Kelvin
U11
R17
121 Ohms
VDUT_Kel_P
AD8421ARZ
R20
47 Ohms
C50
10 µF
C51
0.1 µF
C47
10 pF
-4V
TPH16
HP_Voltage
R22
6.8 kOhms
R21
8.06 kOhms
U14A
R23
3.36 kOhms
C54
10 pF
R24
976 Ohms
C48
0.1 µF
C49
0.1 µF
Low Power InAmp
C52
0.1 µF
C53
10 µF
VDUT-
U13
R26
121 Ohms
VDUT#
TPH17
LP_Voltage
R25
1 kOhms
C55
10 pF
R27
47 Ohms
C56
10 µF
C57
0.1 µF
Heuristic Cascade for Lowpower Mode
TPH18
R29
6.8 kOhms
R28
8.06 kOhms
U12A
R30
4.7 kOhms
C60
470 pF
R31
7.5 kOhms
C61
10 pF
C58
0.1 µF
C59
0.1 µF
R33
6.8 kOhms
R32
8.06 kOhms
U12B
R34
5.11 kOhms
C63
470 pF
R35
8.06 kOhms
C62
10 pF
SW4
SW3
SW2
SW1
SW5
Cascade_SW
R37
6.8 kOhms
R36
8.06 kOhms
U12C
R38
5.11 kOhms
C64
470 pF
R39
8.06 kOhms
C65
10 pF
R41
6.8 kOhms
R40
8.06 kOhms
U12D
R42
5.11 kOhms
C66
470 pF
ADA4622-4ARZ
R43
8.06 kOhms
C67
10 pF
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Laboratory: ETHZ D-ITET PBL
Date: 04/03/2023 16:16:37
Rev: 2
Variation: [No Variations]
Project: Master Thesis
Power Profiler Module
Drawn By: Nando Galliard
Checked By: Federico Villani
File: ppm_cascade.SchDoc
Sheet: 3 / 5

Buffer Stage to ADC



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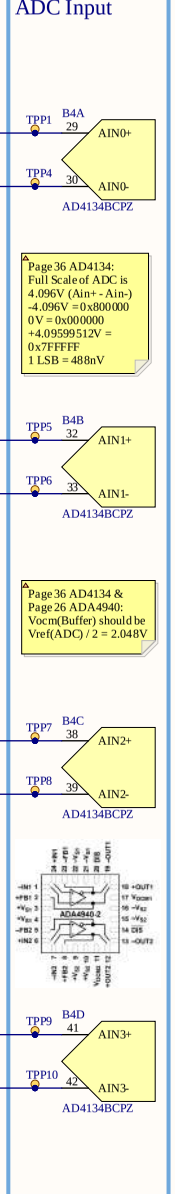
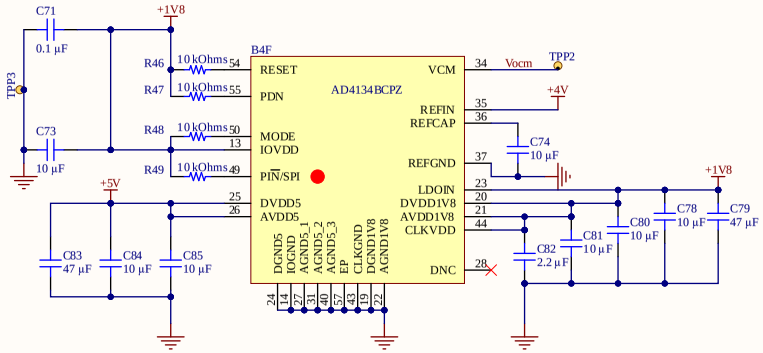
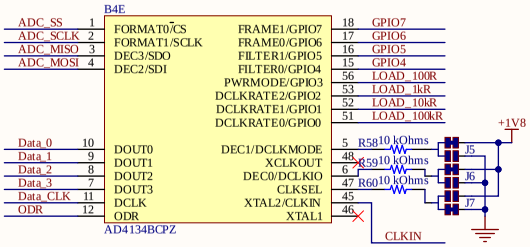


ADC Power

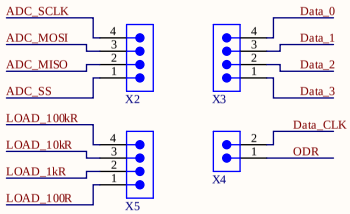
https://www.analog.com/media/en/technical-documentation/evaluation-documentation/eval-ad4134fmcz-layout-file.pdf



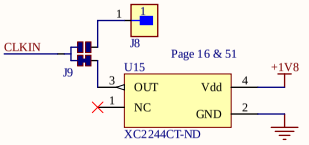
ADC Data Interface



ADC Data Testpoints



ADC Oscillator



ADC Harness

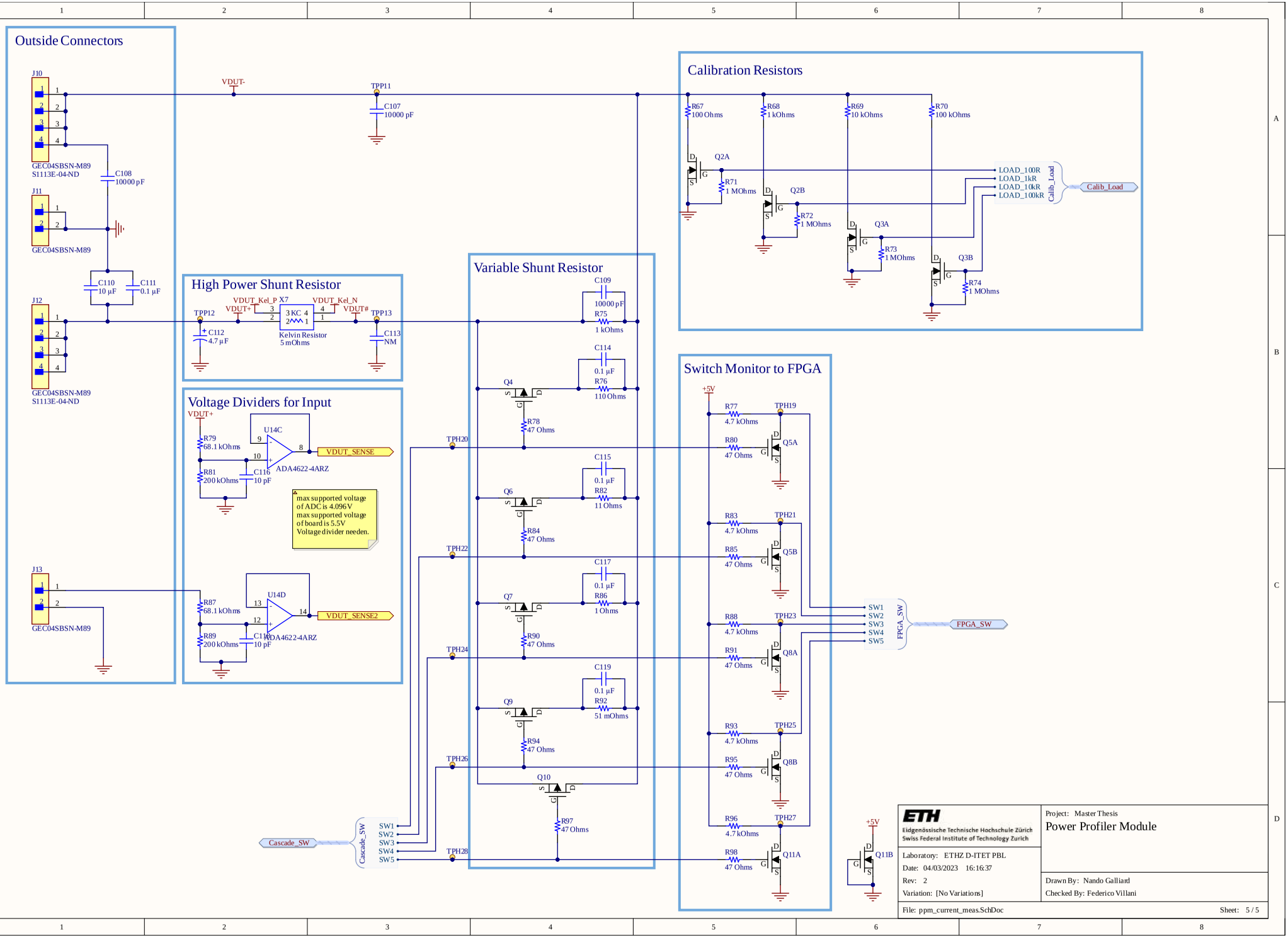
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

Laboratory: ETHZ D-ITET PBL
Date: 04/03/2023 16:16:37
Rev: 2
Variation: [No Variations]

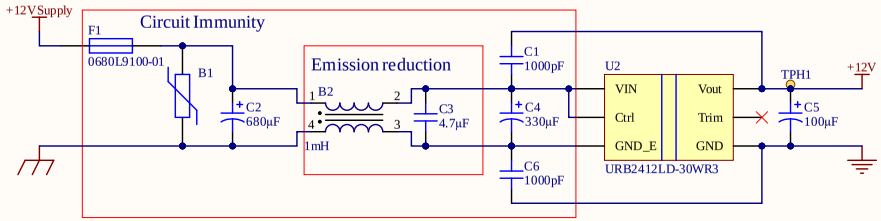
Project: Master Thesis
Power Profiler Module

Drawn By: Nando Galliard
Checked By: Federico Villani

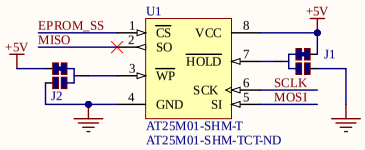
File: ppm_adc.SchDoc
Sheet: 4 / 5

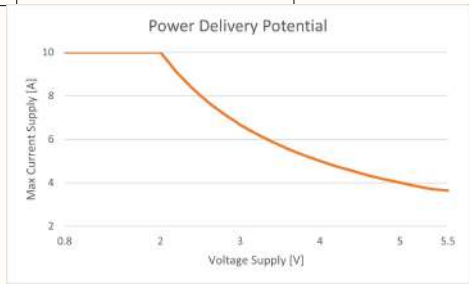

Outside Connectors
J10
GEC04SBSN-M89
S1113E-04-ND
C108
10000 pF
J11
GEC04SBSN-M89
C110
10 µF
C111
0.1 µF
J12
GEC04SBSN-M89
S1113E-04-ND
J13
GEC04SBSN-M89
VDUT-
TPP11
C107
10000 pF
High Power Shunt Resistor
VDUT_Kel_P
VDUT+
X7
VDUT_Kel_N
VDUT#
TPP12
TPP13
3 KC 4
2 1
Kelvin Resistor
5 mOhms
C112
4.7 µF
C113
NM
Voltage Dividers for Input
VDUT+
U14C
R79
68.1 kOhms
R81
200 kOhms
C116
10 pF
ADA4622-4ARZ
VDUT_SENSE
max supported voltage
of ADC is 4.096V
max supported voltage
of board is 5.5V
Voltage divider needen.
U14D
R87
68.1 kOhms
R89
200 kOhms
C118
10 pF
ADA4622-4ARZ
VDUT_SENSE2
Variable Shunt Resistor
C109
10000 pF
R75
1 kOhms
C114
0.1 µF
R76
110 Ohms
Q4
R78
47 Ohms
TPH20
C115
0.1 µF
R82
11 Ohms
Q6
R84
47 Ohms
TPH22
C117
0.1 µF
R86
1 Ohms
Q7
R90
47 Ohms
TPH24
C119
0.1 µF
R92
51 mOhms
Q9
R94
47 Ohms
TPH26
Q10
R97
47 Ohms
TPH28
Cascade_SW
SW1
SW2
SW3
SW4
SW5
Calibration Resistors
R67
100 Ohms
R68
1 kOhms
R69
10 kOhms
R70
100 kOhms
Q2A
R71
1 MOhms
Q2B
R72
1 MOhms
Q3A
R73
1 MOhms
Q3B
R74
1 MOhms
LOAD_100R
LOAD_1kR
LOAD_10kR
LOAD_100kR
Calib_Load
Calib_Load
Switch Monitor to FPGA
+5V
R77
4.7 kOhms
TPH19
R80
47 Ohms
Q5A
R83
4.7 kOhms
TPH21
R85
47 Ohms
Q5B
R88
4.7 kOhms
TPH23
R91
47 Ohms
Q8A
R93
4.7 kOhms
TPH25
R95
47 Ohms
Q8B
R96
4.7 kOhms
TPH27
R98
47 Ohms
Q11A
Q11B
SW1
SW2
SW3
SW4
SW5
FPGA_SW
FPGA_SW
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Laboratory: ETHZ D-ITET PBL
Date: 04/03/2023 16:16:37
Rev: 2
Variation: [No Variations]
Project: Master Thesis
Power Profiler Module
Drawn By: Nando Galliard
Checked By: Federico Villani
File: ppm_current_meas.SchDoc
Sheet: 5 / 5

12V DCDC Isolation

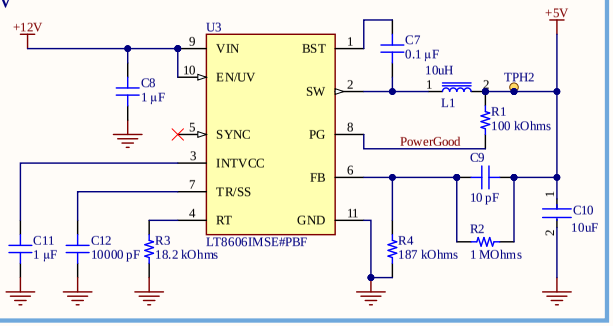


EEPROM

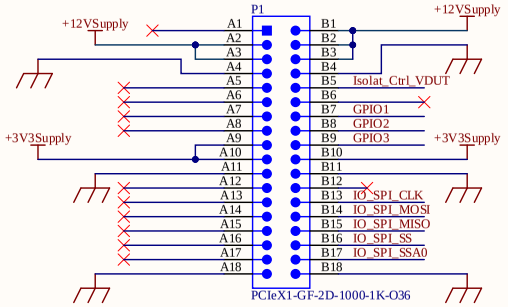




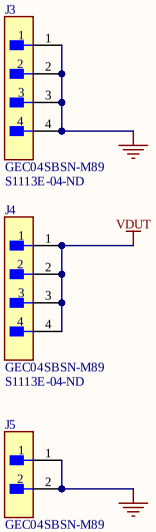
5V



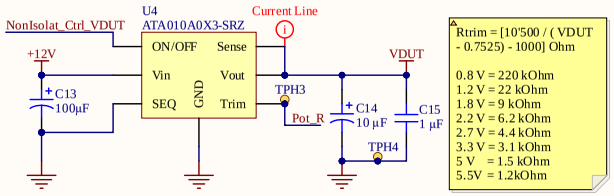
PCI X1 Connector



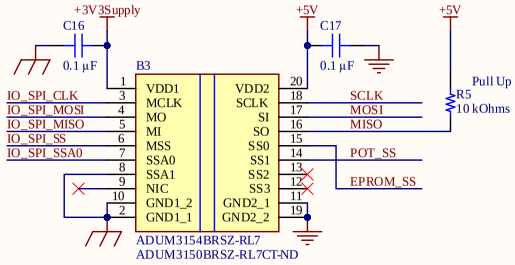
Outside Connectors



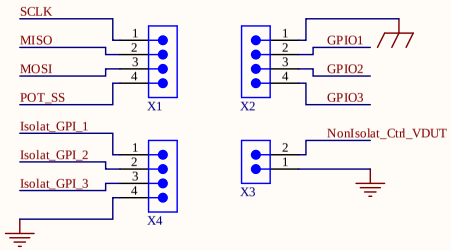
12V / 0.8 to 5.5V DCDC



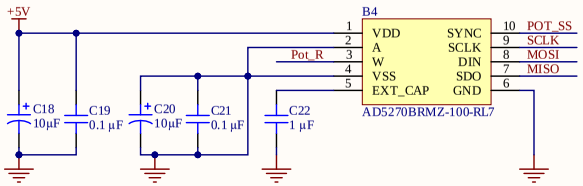
SPI I/O ADC to FPGA



Data Testpoints



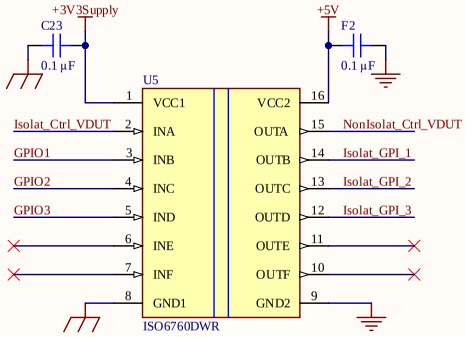
Digital Potentiometer



R_AW (D) = D / 1024 * R_AW
D value from 0x000 to 0x400 in decimal
R_AB = 100 kOhm

Bit	R +/- 1%	V
12	1172	5.5870
13	1270	5.3790
14	1367	5.1881
15	1465	5.0124
18	1758	4.5599
25	2441	3.8036
32	3125	3.2980
37	3613	3.0285
42	4102	2.8107
45	4395	2.6989
51	4980	2.508
59	5762	2.305
64	6250	2.201
76	7422	1.999
83	8105	1.906
92	8984	1.804
133	12988	1.503
230	22461	1.200
424	41406	1.000

Data-In to Module



M1 Mounting Hole M2.5
M2 Mounting Hole M2.5

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

Project: Master Thesis
Power Delivery Module

Laboratory: ETHZ D-ITET PBL
Date: 04/03/2023 13:45:14
Rev: 1
Variation: [No Variations]

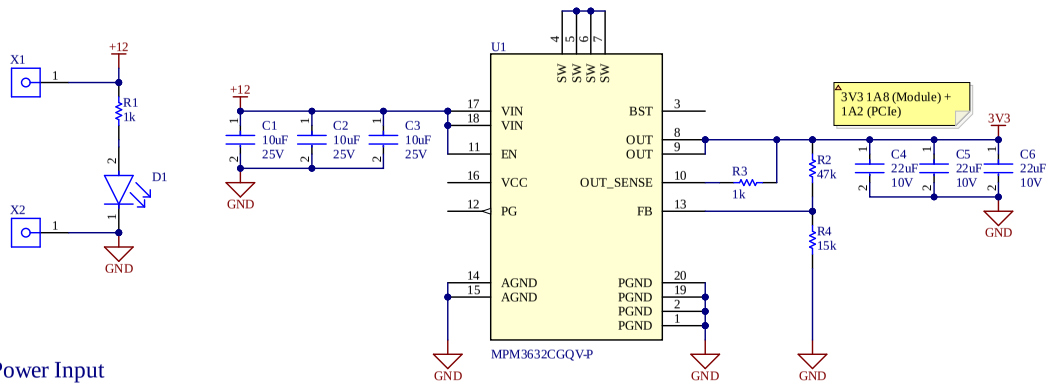
Drawn By: Nando Galliard
Checked By: Federico Villani

File: pdm_1.SchDoc
Sheet: 1 / 1

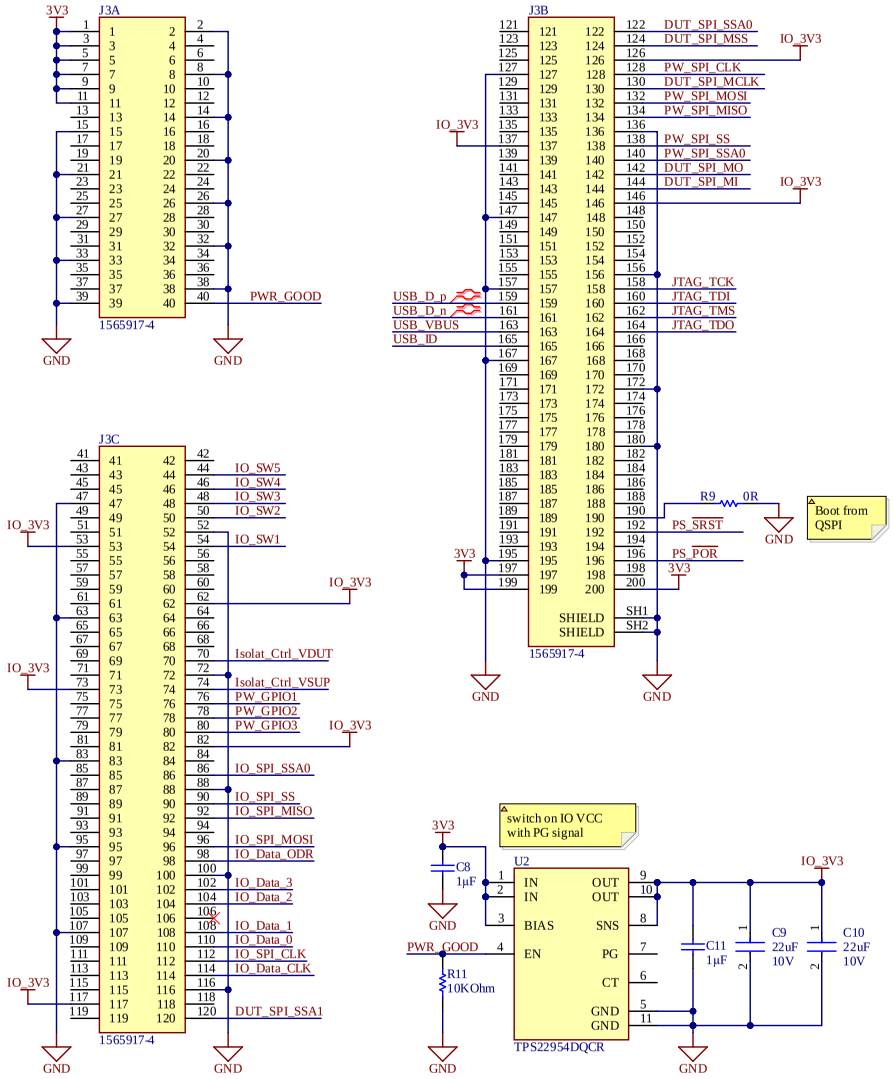
ETHZurich

Logo ETH Zurich

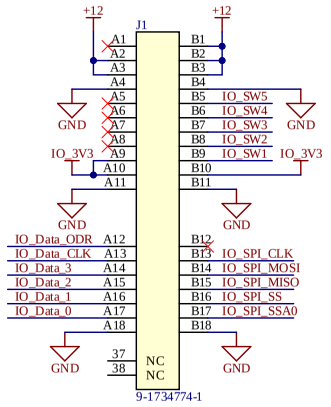
Power Input



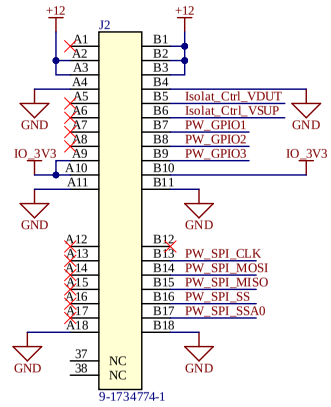
FPGA



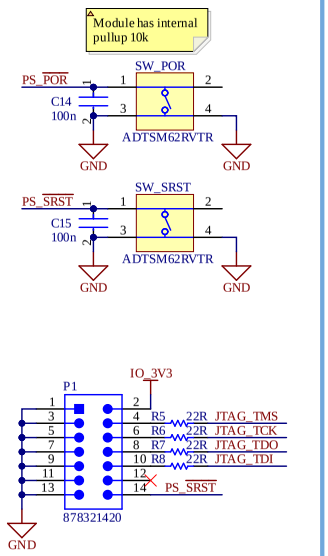
Sensing Module



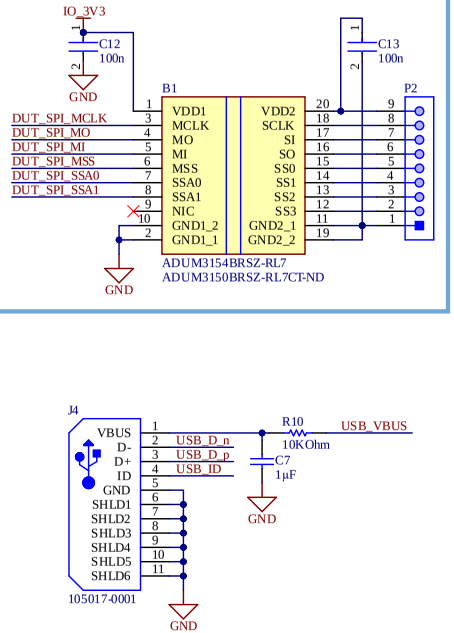
Power Module



FPGA Reset and Programming



Sensor Interface



Mounting Holes

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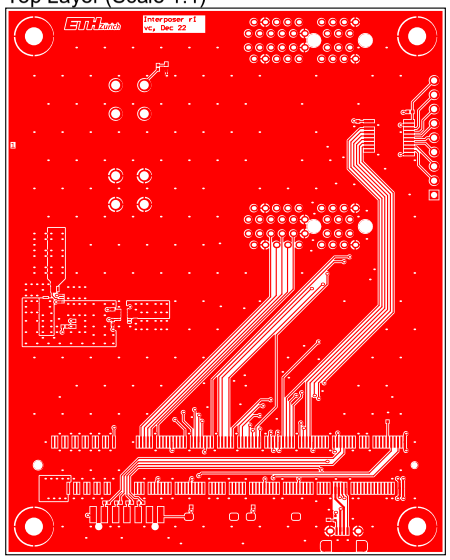
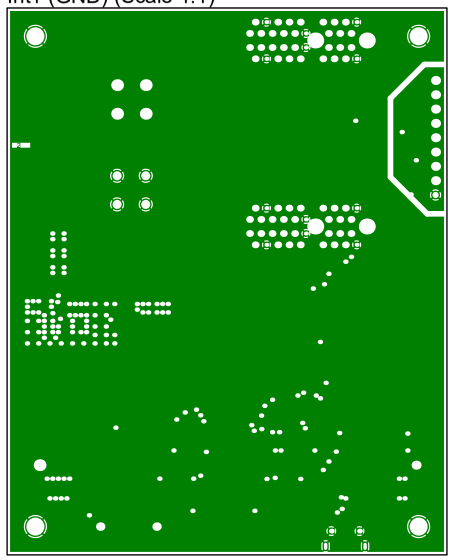
Drawing number: 1	Rev: r1	Format: A3		Laboratory: PBL	Sheet: Interposer.SchDoc
Date: 09/12/2022 16:59:35				Drawn by: Ch. Vogt	Page 1 of 1
File: C:\Repository\MT_Boardfiles\Interposer\Interposer.SchDoc					

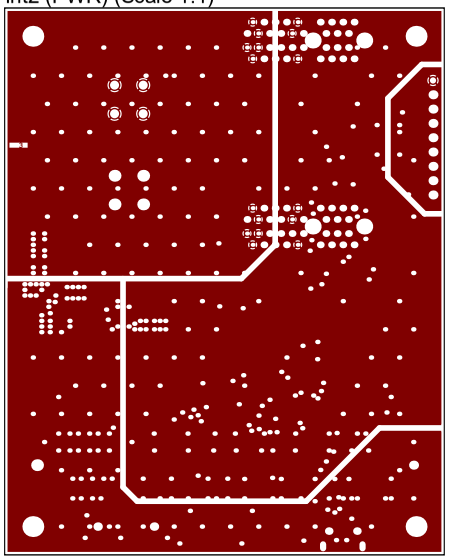
Top Layer (Scale 1:1)



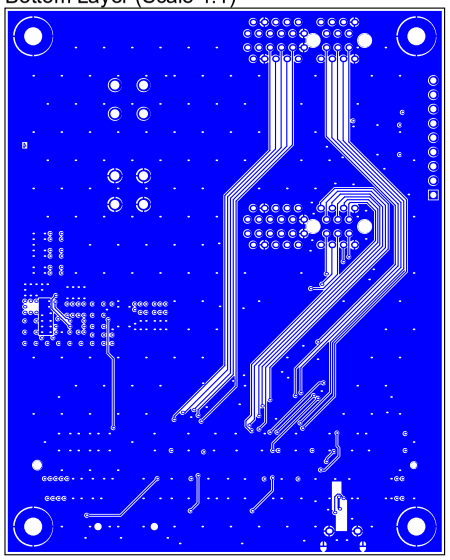
Int1 (GND) (Scale 1:1)



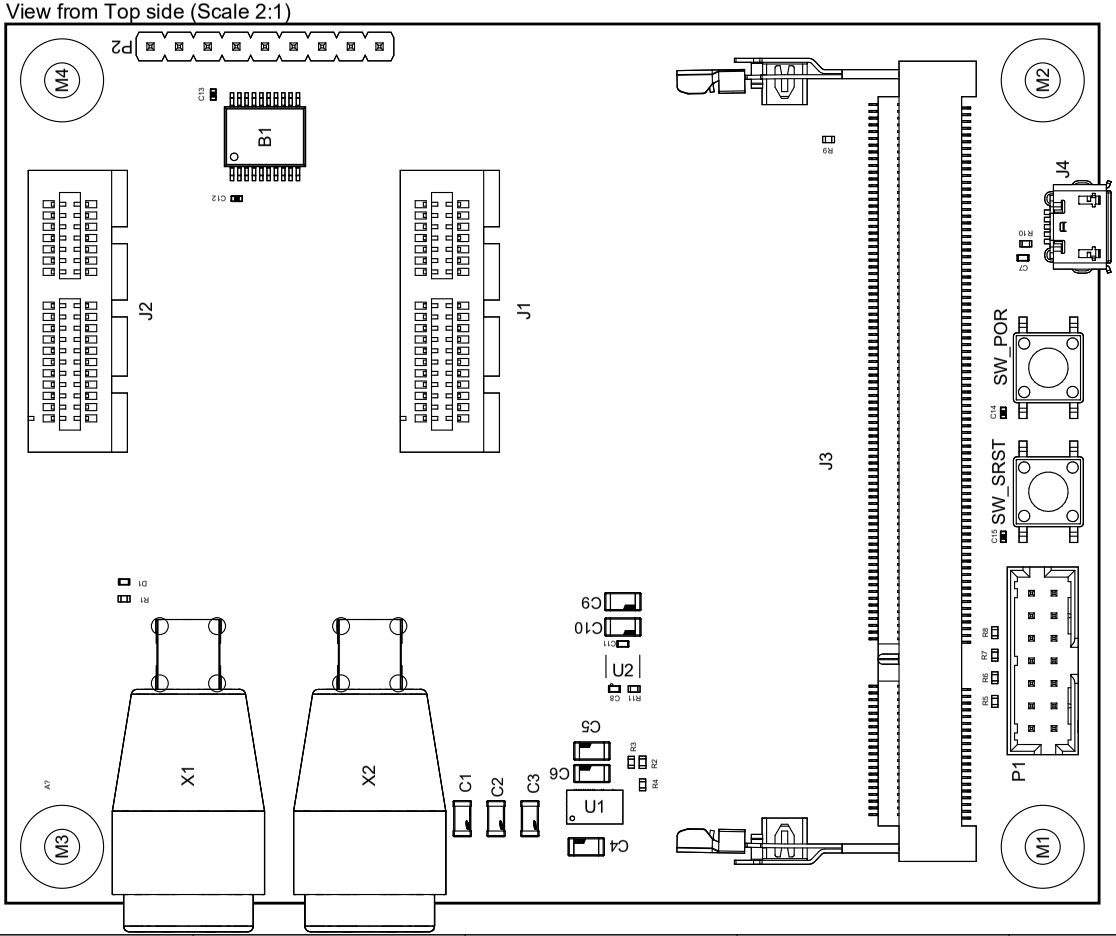
Int2 (PWR) (Scale 1:1)



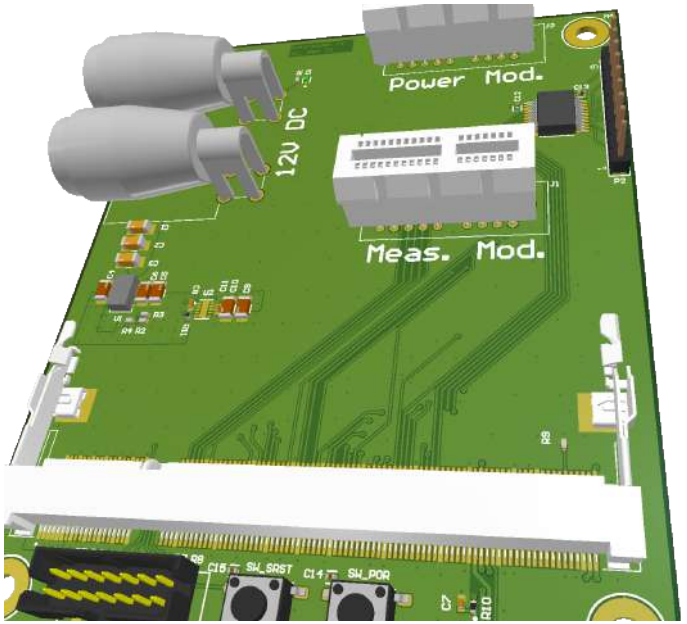
Bottom Layer (Scale 1:1)



View from Top side (Scale 2:1)

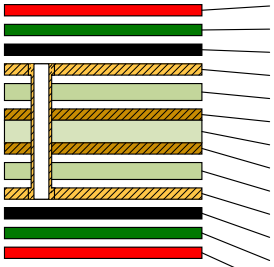


Realistic View



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich			Project: **Interposer Board PowerTracer**
Drawing number: 1	Rev: r1	Format: **A3**	LaboratoryPBL
Date: 09/12/2022 16:59			Drawn by: Ch. Vogt
File: C:\Repository\MT_Boardfiles\Interposer\Draftsman\int_ASM.PCBDwf			Sheet: int_ASM.PCBDwf Page 1 of 1

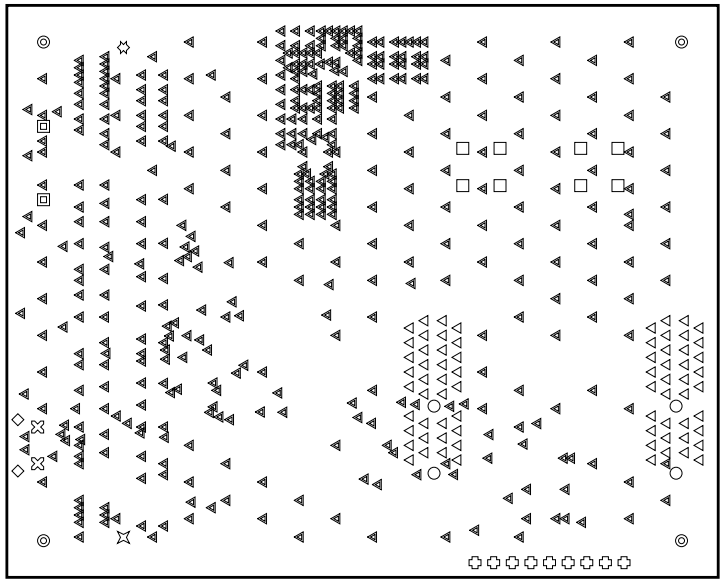
Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.002mm	SM-001	Solder Mask	GTS
PbSn	Top Surface Finish	0.004mm		Surface Finish	
CF-004	**Top Layer**	**0.035mm**		**Signal**	**GTL**
Prepreg		*0.110mm*	*PP-017*	*Dielectric*	
CF-004	**Int1 (GND)**	**0.035mm**		**Internal Plane**	**GP1**
Core		*0.800mm*	*Core-039*	*Dielectric*	
CF-004	**Int2 (PWR)**	**0.035mm**		**Internal Plane**	**GP2**
Prepreg		*0.110mm*	*PP-017*	*Dielectric*	
CF-004	**Bottom Layer**	**0.035mm**		**Signal**	**GBL**
PbSn	Bottom Surface Finish	0.004mm		Surface Finish	
Surface Material	Bottom Solder	0.002mm	SM-001	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.172mm

Drill Drawing View (Scale 1.3:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair	Via / Pad
▽	457	0.30mm	Plated	Top Layer - Bottom Layer	Via
◇	2	0.60mm	Plated	Top Layer - Bottom Layer	Pad
▽	72	0.71mm	Plated	Top Layer - Bottom Layer	Pad
⊠	2	0.85mm	Plated	Top Layer - Bottom Layer	Pad
⧈	2	1.00mm	Non-Plated	Top Layer - Bottom Layer	Pad
⊠	1	1.10mm	Non-Plated	Top Layer - Bottom Layer	Pad
✣	9	1.10mm	Plated	Top Layer - Bottom Layer	Pad
✡	1	1.60mm	Non-Plated	Top Layer - Bottom Layer	Pad
□	8	1.60mm	Plated	Top Layer - Bottom Layer	Pad
○	4	2.34mm	Non-Plated	Top Layer - Bottom Layer	Pad
◎	4	3.20mm	Plated	Top Layer - Bottom Layer	Pad
	562 Total				

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory: ETHZ D-ITET PBL
Date: 09/12/2022 16:59
Rev: =revision
Variation[No Variations]

Project: =ProjectTitle
*
=Desc1
=Desc2
=Desc3
=Desc4

Drawn By:*
Checked By*

File: =DocumentName

Sheet: 1 / 1

Glossary

main In the SPI protocol, the main device is the orchestrator of the data transfers.

second In the SPI protocol, the second device is subordinate to the main device and is addressed via a second select line dedicated to this second.

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